STRATEGIC & SPECTRUM MISSIONS ADVANCED RESILIENT TRUSTED SYSTEMS (S^{2}MARTS)
REQUEST FOR SOLUTIONS (RFS)

in support of the

Rapid Assured Microelectronics Prototypes – Commercial (RAMP-C)

Project No. 21-07

All prospective respondents must be members of the NSTXL consortium.

1. **Project Title:** Rapid Assured Microelectronics Prototypes – Commercial (RAMP-C)

2. **Prototype Project Sponsor/Requiring Activity:** Naval Surface Warfare Center (NSWC) Crane Division, Trusted Microelectronics Division (GXV)

3. **Contracting Activity:** Naval Surface Warfare Center, (NSWC), Crane Division, Code 0221

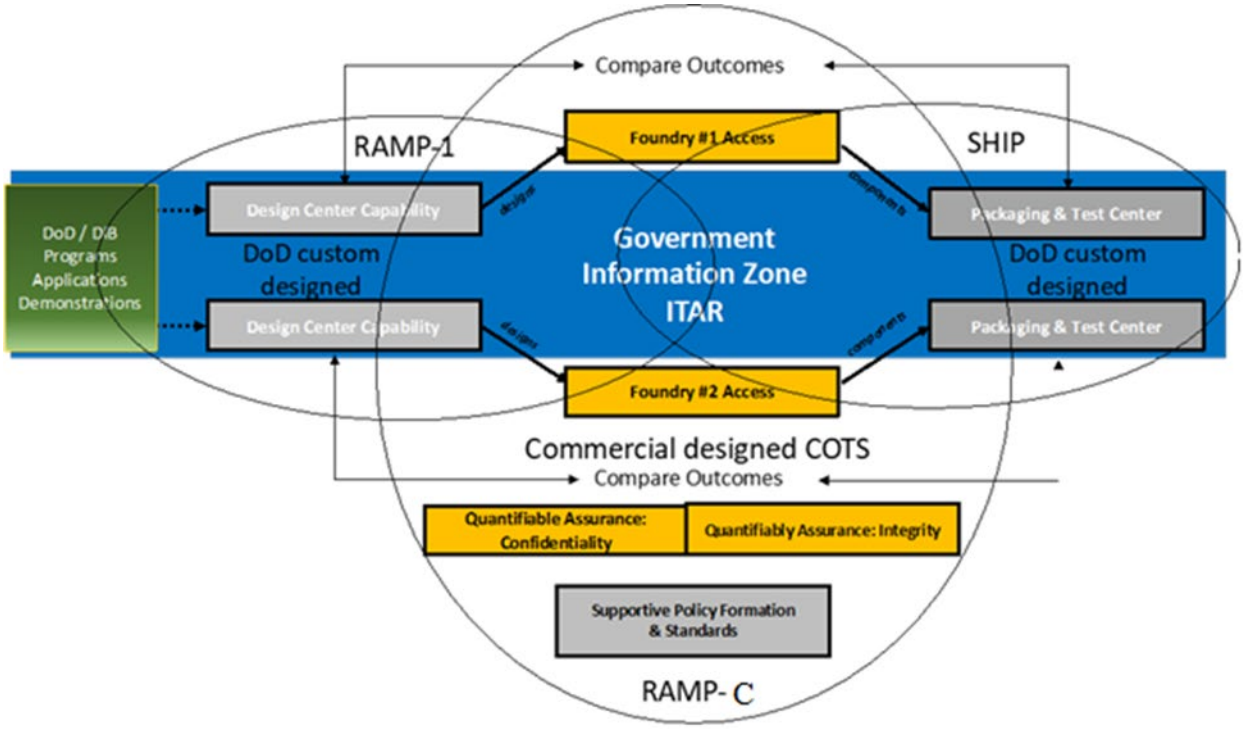
4. **Project Background & Current Capability:**

The United States currently has no onshore access to foundry technology capable of meeting the Department of Defense's (DoD) long-term leading-edge[1] microelectronics manufacturing needs. Most United States (U.S.) microelectronics design companies are fabless, meaning that these companies design and sell integrated circuits through outsourcing their fabrication to a specialized manufacturer called a semiconductor foundry. These foundries are typically, but not exclusively, located in Asia, primarily in Taiwan and South Korea. Fabless companies benefit from lower capital costs while concentrating their research and development resources on the end market. TSMC supplies 89% of the world's most advanced Silicon Complementary Metal-Oxide Semiconductor (Si CMOS) integrated circuits fabricated using technology more advanced than the 40nm node, and produces those chips exclusively in Taiwan. There is currently no commercially viable option, which will provide a U.S. located leading-edge foundry that can fabricate the assured leading-edge custom and integrated circuits and Commercial off the Shelf (COTS) products required for critical DoD systems. The purpose of the RAMP-C program is to develop such an option.

Two existing Office of Secretary Defense Research & Engineering (OSD R&E) programs are critical and complementary to the RAMP-C program: Rapid Assured Microelectronics Prototypes using Advanced Commercial Capabilities (RAMP) and digital State of the Art

[1] For the purposes of this RFS, "leading edge" is defined as a digital CMOS node ≤ 7nm.

Heterogeneous Integrated Packaging (SHIP). Jointly SHIP, RAMP, and RAMP-C will address the entire Microelectronics design/manufacturing cycle as illustrated in Figure 1. RAMP addresses the critical process of physical design (also called back-end design) that transforms a high-level programming form register-transfer level (RTL) of a design into the complex, technology specific polygon form of a design that is required as input for the wafer fabrication process. RAMP facilitates DoD use of advanced commercial design capabilities. SHIP will develop the capability to use advanced commercial heterogeneous integration and advanced packaging technology to package and test the integrated circuits designed in RAMP and fabricated in the leading edge commercial facility developed in RAMP-C. All three programs will assure access to advanced capabilities in facilities located in the U.S. Confidentiality and integrity of commercial and DoD designs will be assured through the use of Quantifiable Assurance methods across all three programs.



Collectively, the three programs, SHIP, RAMP, and RAMP-C display the following critical characteristics:

1. Ensures DoD access through leveraging U.S. located, commercially developed technology that is made viable through extensive use by high-volume commercial companies.

2. Measurably assures the confidentiality and integrity of DoD leading edge integrated circuits through use of Quantifiable Assurance methods integrated across the microelectronic design/manufacturing enterprise.
3. Facilitates use of advanced integrated circuit technology by the Defense Industrial Base (DIB) by leveraging learning from best-in-class commercial partners.

5. Desired End-State Objective(s) & Success Criteria:

This RFS project award will encompass Phase 1 only, establishment of the design and fabrication infrastructure for DoD dual use commercial prototypes. Subsequent phases, Phase 2 (Full design of product prototypes and fabrication of product test chips) and Phase 3 (Fabrication and increased yield of full product prototypes) may be funded and executed upon successful completion of Phase 1, but are outside the scope of this RFS. If funded, Phase 2 and Phase 3 may be accomplished via a procurement contract or Other Transactions (OT) agreement, which will be determined at that time. Phase 1 transactions will be awarded in sub-phases valued at less than $100M. Award of each subsequent sub-phase will be dependent upon the successful completion of the previous sub-phase. Therefore, in accordance with the Under Secretary of Defense Memorandum dated 20 NOV 2018, Authority for Use of Other Transactions for Prototype Projects under 10, United States Code, Section 2371b, higher level approval authorities will not be required. Successful completion of Phase 1 will be measured via the metrics identified within the deliverables table below.

Sub-Phase 1a – Planning Phase ($75M)

- Task 1: Develop Process Design Kit (PDK) requirements and customer support strategy
- Task 2: Develop Foundational intellectual property (IP) requirements and development plan
- Task 3: Develop critical 3rd party IP requirements and development plan
- Task 4: Develop test chip requirements and development plan
- Task 5: Development yield ramp/capacity requirements and development plan

Sub-Phase 1b – IP Foundation Phase ($75M)

- Task 1: Develop initial proto-type PDK with initial customer support plan
- Task 2: Develop initial Foundational IP
- Task 3: Develop initial critical 3rd party IP
- Task 4: Develop test chip high-level design
- Task 5: Development yield ramp/capacity detailed plan

Sub-Phase 1c – Design Phase ($84M)

- Task 1: Upgrade PDK, share production data and refine customer support
- Task 2: Full build-out of Foundational IP

- Task 3: Refine first 3rd party IP proto-type deliverable
- Task 4: Test chip detailed design
- Task 5: Test chip yield ramp plan

Sub-Phase 1d – Design Transition Phase ($75M)

- Task 1: Finalize PDK and customer support infrastructure
- Task 2: Finalize Foundational IP proto-type deliverable
- Task 3: Finalize first 3rd party IP proto-type deliverable
- Task 4: Finalize test chip detailed design
- Task 5: Finalize test chip yield ramp plan

The expectation is that successful completion of all three program phases will result in a U.S. located, commercially viable, leading-edge logic foundry eco-system that will be available for commercial and DoD use. This leading-edge logic foundry ecosystem will incorporate Quantifiable Assurance standards to measurably assure DoD custom and DoD critical COTS integrated circuits. Achievement of this goal will require strong commercial collaboration between multiple fabless companies, 3rd party design module (IP) providers, and a U.S. located foundry capable of complex System on a Chip (SoC) fabrication using 7nm/5nm Si CMOS technology.

Phase 1 Objectives (18 months):

The Navy seeks to develop the eco-system for a leading-edge foundry located in the U.S. and enable implementation of Quantifiable Assurance standards for DoD custom integrated circuits and critical dual use COTS products. At the end of Phase 1 it is expected that the fabless companies and the leading-edge foundry will have instituted bilateral commercial agreements, or exhibit a timeline to establish those agreements for manufacturing that ensure long-term viability of the foundry capability and that will include key performance terms. Phase 1 will be achieved through 5 major objectives:

1. Establishment of a strong, customer-focused design enablement organization that provides complete, well documented, and verified design enablement including a PDK that supports design of high-volume, complex SoCs by fabless companies and by DoD/DIB.
2. Provision of required foundation IP (core logic libraries, static random access memory (SRAM) compilers, General Purpose inputs and outputs, eFuse blocks) developed and verified in the target fabrication technology.
3. Provision of 3rd party IP that is required to support Phase 1 design of the fabless company product-based test chips and establishment of an aligned Phase 1&2 schedule for development of all 3rd party IP required for the initial commercial products designed by fabless companies.
4. Design of multiple test chips that are based on eventual product needs and are intended to provide added confidence in the ability of the leading-edge foundry to meet fabless company targets for Power, Performance, Area (PPA), and yield.
5. Definition of the detailed plan, schedule, and budget required to provide the

required wafer fabrication capacity/yield during Phases 2&3.

Each of these objectives is described in more detail below:

1. Foundry Design Enablement

   The objective will be to establish a world-class set of design enablement components and the responsive customer design support organization required to support implementation of those components by customer design teams. Design enablement will support the leading-edge Si CMOS technology implemented by the U.S. located foundry and will include all of the components required to design advanced, complex SoCs: e.g. multiple Vt transistor models, interconnect extraction technology files, design rule checks (DRC) decks, reliability models, transistor ageing models, SRAM bit cells, eFuse elements, standard P-Cells, layer fill decks, and mask layer coloring software. The enablement will be verified with hardware and will provide the insight and data required to implement the Quantifiable Assurance method for DoD critical integrated circuits. The design enablement task will also provide the guidance required for fabless companies to use the enablement components to design best-in-class SoCs. The design enablement should support the multiple design flows implemented by the lead fabless company designs. This task must be performed by the leading-edge foundry proposer.

2. Foundation IP

   The objective will be to design and document the Foundation design elements (IP) required for fabless company teams to design advanced, complex SoCs. Example of these design elements are: a standard cell logic library, a set of SRAM memory compilers, selected General Purpose Input/Output (I/O) modules, and eFuse controller modules. Each of these foundation IP elements can be provided either by the foundry or by a 3rd party provider, depending on the appropriate commercial arrangements. In either case, the foundation IP must be fully verified through testing of hardware and must meet the quality standards required by fabless design companies. The provider of the Foundation IP must also provide the insight and data required to implement the Quantifiable Assurance method for DoD critical integrated circuits. This task may be performed by the leading-edge foundry proposer or a 3rd Party IP proposer.

3. 3rd Party IP

   The objective will be to design and document the 3rd party design modules (IP) required for fabless company teams to design advanced test chips and products proposed in Task 4. These modules are generally more complex than those provided as a part of Foundation IP and are built using the foundry-provided enablement and Foundry IP. Although each fabless company design requires

unique design modules, there are common 3rd party IP modules that are generally available for fabless companies to use in their designs. Examples of this common 3rd party IP are: memory controller modules, standard phase lock loops (PLLs), standard analog to digital and digital to analog converter (ADC/DAC) modules, and universal serial bus input/output (USB I/O). This task will also require coordination with both the fabless and foundry participants to define the appropriate list of 3rd party IP that is required across the fabless company requirement list. The 3rd party IP provider will also develop a consensus regarding the format and delivery of 3rd party IP design files and documentation to the fabless company design teams. The 3rd party IP must be fully verified through testing of hardware and must meet the quality standards required by fabless design companies. The providers of the 3rd party IP must also provide the insight and data required to implement the Quantifiable Assurance method for DoD critical integrated circuits. This task may be performed by a 3rd party IP proposer or a fabless company design team.

4. Test chip design

   The objective will be to design the test chips that will support the individual fabless company SoC products that will be designed during Phase 2 and fabricated in Phase 3. Test chip design will be complete before the end of Phase 1 to enable the start of fabrication at the beginning of Phase 2. It is expected that three different products from three different fabless companies will be selected for implementation in the RAMP-C program. These companies must have demonstrated capability to design and productize high volume microelectronics components at leading-edge nodes. Each of those three companies will design a test chip during Phase 1 and each test chip should provide the fabless company design team with hardware verification of critical aspects of final product design including mixed-signal performance. Design and fabrication of the test chips are also intended to provide added confidence in the ability of the leading-edge foundry to meet fabless company targets for PPA and yield. This task must be performed by a set of fabless company design teams.

5. Foundry yield/capacity plan

   The objective will be to develop the detailed plan, schedule, and budget required to provide the required wafer fabrication capacity and yield that will be implemented during Phase 2 and Phase 3. The plan will include a detailed schedule for availability of fabrication capacity for processing of fabless company test chip and product designs. The plan will include a schedule for building construction, equipment installation, equipment qualification, integrated process qualification, production Si wafer starts, and available production Si capacity. The plan will also include availability of fabrication capacity for fabless company use before the eventual program-developed fabrication capacity is in place. This

task will also provide a test chip and product yield ramp schedule based on process yield and expected defect density. This task will also provide a month-by-month budget associated with the planned capacity and yield ramps. Finally, this task will develop a plan to achieve commercial viability developed jointly by the leading-edge foundry and fabless design companies.

Phase 2 Objectives (12 months)

The major objective of Phase 2 is to begin successful implementation of plans developed during Phase 1. Specific implementation expectations include:

1. Demonstration of successfully meeting the milestones for foundry capacity and yield ramps.
2. Fabrication and evaluation of fabless company-designed test chips.
3. Design of fabless company full product SoCs.
4. Development of the on-schedule Foundation and 3rd party IP ecosystem required for fabless company product designs.
5. Continual improvement of foundry design enablement infrastructure.
6. Implementation of a Quantifiable Assurance data provision plan for the design and fabrication flows.
7. Implementation start of the established commercial viability plan including initial bilateral commercial agreements that include performance-based commitments between the leading-edge foundry and fabless companies.

Phase 3 Objectives (12 months)

The major objective of Phase 3 is to successfully complete implementation of plans developed during Phase 1 and to be prepared for the volume ramp of the fabless company products in a commercially viable manner. Specific implementation expectations include:

1. Capacity in place to fabricate at the level of 26,000 wafer starts per month in foundry capacity at the 7nm/5nm technology node.
2. Demonstration of meeting yield targets for the technology.
3. Commercial qualification of fabless company products, including implementation of the aligned Quantifiable Assurance plan.
4. Development of an expanded 3rd party IP portfolio for future commercial and DoD custom designs.
5. Full implementation of the commercial viability plan including bilateral commercial agreements that include volume commitments by the foundry and fabless companies.

The below table reflects the program schedule.

Table 1: Prototype Project Phase Schedule

Phase	Duration
Phase 1	**18 months** • *Initial Operating Capability (IOC) @ month 6* • *Full Operating Capability (FOC) @ month 18*
Phase 2	**12 months**
Phase 3	**12 months**

6. Project Deliverables

No.	Title of Deliverable	Description (Purpose of Deliverable)	Delivery Frequency	Delivery Method or Location
1	Phase 1a formal briefing: • Task 1: Process Design Kit (PDK) requirements and customer support strategy • Task 2: Foundational intellectual property (IP) requirements and development plan • Task 3: Critical 3rd party IP requirements and development plan • Task 4: Test chip requirements and development plan • Task 5: Yield ramp/capacity requirements and development plan	Understand the requirements and strategy to address for Foundry, Foundation IP, 3rd Party IP and Fabless Company	1/Once	No Later Than Three (3) months from project award.
2	Phase 1b technical report; • Task 1: Initial proto-type PDK with initial customer support plan • Task 2: Initial Foundational IP • Task 3: Initial critical 3rd party IP	Technical reporting on project progress and challenges for Foundry, Foundation IP, 3rd Party IP and Fabless Company	1/Once	No Later Than Twelve (12) months from project award.

No.	Title of Deliverable	Description (Purpose of Deliverable)	Delivery Frequency	Delivery Method or Location
	• Task 4: Test chip high-level design • Task 5: Yield ramp/capacity detailed plan			
3	Interim Phase 1c formal briefing; • Task 1: Upgrade PDK, share production data and refine customer support • Task 2: Full build-out of Foundational IP • Task 3: Refine first 3rd party IP proto-type deliverable • Task 4: Test chip detailed design • Task 5: Test chip yield ramp plan	Update on progress toward final deliverables for Foundry, Foundation IP, 3rd Party IP and Fabless Company	1/Once	No Later Than Fifteen (15) months from project award.
4	Final Phase 1d Delivery comprised of the following elements: • Task 1 Functional PDK • Task 1 Final report describing the customer support organization, evidence of enablement alignment with fabless companies and IP providers, and schedule for continued enablement improvement • Task 5 Detailed foundry capacity and yield plans for Phases 1&2	Foundry	1/Once	No Later Than Eighteen (18) months from project award.
5	Final Phase 1d Delivery comprised of the following elements for Task 2: • Initial set of Foundation IP design collateral and Quantifiable Assurance data • Final report reporting the results of Phase 1 work, a description of the plan for delivery of complete Foundation IP in Phases 2 and 3, as well as evidence of Foundation IP schedule alignment with fabless companies and the foundry	Foundation IP Provider	1/Once	No Later Than Eighteen (18) months from project award.

No.	Title of Deliverable	Description (Purpose of Deliverable)	Delivery Frequency	Delivery Method or Location
6	Final Phase 1d Delivery comprised of the following elements for Task 3: • Initial set of 3rd Party IP design collateral and Quantifiable Assurance data • Final report reporting the results of Phase 1 work, a description of the plan for delivery of complete 3rd Party IP in Phases 2 and 3, as well as evidence of 3rd Party IP schedule alignment with fabless companies and the foundry	3rd Party IP Provider	1/Once	No Later Than Eighteen (18) months from project award.
7	Final Phase 1d Delivery comprised of the following elements for Task 4: • Final test chip design review including delivery of Quantifiable Assurance data and results of the final internal tapeout design review. • Final report reporting the results of Phase 1 work, the plan for testing and evaluation of the test chip in Phase 2, a plan for delivery of complete full product design in Phase 2, and plans for qualification of the product in Phase 3	Fabless Company	1/Once	No Later Than Eighteen (18) months from project award.
8	Phase 1 Technical Interchange Meeting (TIM) and Meeting Minutes		18/Monthly	Five (5) business days after end of previous month

7. Current Project Budget: $310,000,000

This value represents what is currently available for the subject project at the time of the RFS release. This value is subject to change but is being provided for planning purposes. Respondents should propose a cost that reflects the respondent's approach and not use the budgetary estimate only. Respondents are encouraged to clearly explain how much of their solution can be developed for the advertised amount or a lesser amount. Capabilities or project phases that will require additional funding beyond the project budget must be identified at Section 10(b)(iii)(6) herein.

This value represents what is currently available for the subject project across all performers for Phase 1 at the time of the RFS release. An initial estimate that indicates a breakdown between tasks is shown below.

Task 1, (Sub-phase 1a-1d): $10,000,000
Task 2, (Sub-phase 1a-1d): $50,000,000
Task 3, (Sub-phase 1a-1d): $100,000,000
Task 4, (Sub-phase 1a-1d): $20,000,000 per product design (3 designs)
Task 5, (Sub-phase 1a-1d): $90,000,000

Respondents should propose a Firm-Fixed Price (FFP) for sub-phase 1a. A Rough Order of Magnitude (ROM) should be proposed for the remaining sub-phases.

Sub-Phase 1a – Planning Phase ($75M)

- Task 1: Develop Process Design Kit (PDK) requirements and customer support strategy
- Task 2: Develop Foundational intellectual property (IP) requirements and development plan
- Task 3: Develop critical 3rd party IP requirements and development plan
- Task 4: Develop test chip requirements and development plan
- Task 5: Development yield ramp/capacity requirements and development plan

Sub-Phase 1b – IP Foundation Phase ($75M)

- Task 1: Develop initial proto-type PDK with initial customer support plan
- Task 2: Develop initial Foundational IP
- Task 3: Develop initial critical 3rd party IP
- Task 4: Develop test chip high-level design
- Task 5: Development yield ramp/capacity detailed plan

Sub-Phase 1c – Design Phase ($84M)

- Task 1: Upgrade PDK, share production data and refine customer support
- Task 2: Full build-out of Foundational IP
- Task 3: Refine first 3rd party IP proto-type deliverable
- Task 4: Test chip detailed design
- Task 5: Test chip yield ramp plan

Sub-Phase 1d – Design Transition Phase ($75M)

- Task 1: Finalize PDK and customer support infrastructure
- Task 2: Finalize Foundational IP proto-type deliverable
- Task 3: Finalize first 3rd party IP proto-type deliverable
- Task 4: Finalize test chip detailed design
- Task 5: Finalize test chip yield ramp plan

8. Security Classification, Respondent Restrictions, and other required compliances:

This RFS has been released under the following—

☒Distribution Statement A: *Approved for public release.*

This project encompasses the following restrictions:

a. Security Classification: Secret clearance is not required at time of award, but may be required during execution or in future phases.

b. ITAR Compliance is not required at time of proposal submission

c. Respondent Restrictions: A respondent is not required to be a US owned company to propose on this effort, but must be located within the US.

d. Respondents shall complete the Section 889(a)(1)(B) Prohibition on Contracting with Entities Using Certain Telecommunications and Video Surveillance Services or Equipment representation attached to this RFS (Attachment #1), and return the signed representation with the submitted proposal.

9. Level of Data Rights Requested by the Government:

☒ Government Purpose Rights: The right to use, modify, reproduce, release, perform, display, or disclose technical data within the Government without restriction. This also includes the rights to release or disclose technical data outside the Government and authorize persons to whom release or disclosure has been made to use, modify, reproduce, release, perform, display, or disclose technical data for United States government purposes. This level of restriction is set at five-years but may be negotiated & tailored to a specific project. The five-year period, or such other period that may be negotiated, would commence upon

execution of the agreement that required development of the items, components, or processes or creation of the data. The performer will have the exclusive right, including the right to license others, to use technical data in which the Government has obtained government purpose rights under this agreement for any commercial purpose during the five-year period. Upon expiration of the five-year period (or other negotiated length of time), the Government will receive unlimited rights in the technical data and computer software.

At a minimum, the Government is requesting the delivery of all intellectual properties (IPs) developed during the project. The performer shall deliver all the CAD and EDA files, including scripts, RTL, HDL, netlists, simulation files (e.g., MATLAB, ADS, SPICE, Cadence, Synopsys, Mentor Graphics, etc.), testbenches, schematics, layouts (e.g. GDS, mask-ready GDS, etc.), design databases, timing information, and mechanical drawings of the Integrated Circuits and Systems; algorithms; test assemblies; all package design and drawings (schematics, layouts, etc.); the PCB/module test/evaluation board designs, schematics, bill of materials (BOMs), and drawings; full design and verification projects, testbenches, and behavioral and functional models for all IPs' functions and operations; comprehensive reports and documentation including information for future IP re-use by another party; comprehensive reports including the principles of function, operation, performance, design methodologies and choices, verification methodologies and choices; hierarchical list identifying all ancillary/building blocks, foundation IP, functional IP, and verification IP; list and versions of all EDA/CAD tools, internal tools, methodologies, scripts, and PDK versions; all design review (e.g. PDR, CDR, FDR, etc.) documents; interfacing of the designs of the integrated circuits and systems along with detailed test and verification plans and developed supporting software; engineering support; and performing hardware prototypes/test articles demonstrating capabilities. The performer shall ensure that all IPs are licensed appropriately including the complete transfer/transition to the Government. The performer shall deliver above items no later than 1 month after the completion of effort. All of these requests should be incorporated in the easy-to-use, data-driven database for use by a novice circuit designer.

10. RFS and Response Process:

a. The following is requested from all respondents:

Proposal Volumes	Page Limitation
Technical Report	40 pages (max)
Price Response	5 pages (max)

For written submissions, the following formatting guidelines shall be followed by respondents:

- 10-point font (or larger) for all response narratives; smaller type may be used in figures and tables but must be clearly legible.

- Single-spaced, single-sided (8.5 by 11 inches).
- Margins on all sides (top, bottom, left, and right) should be at least 1 inch.
- Page limitations shall not be circumvented by including inserted text boxes/pop-ups or internet links to additional information. Such inclusions are not acceptable and will not be considered as part of the response
- Files must be submitted in PDF and/or Microsoft Word formats only. Price volumes may be submitted in an editable, unlocked Excel file

b. Each submittal **must include** (i) a Cover Page, (ii) a Technical Response, and (iii) a Price Response that each align to the instructions below:

i. Cover Page: (Not included within page count) The cover page shall include the company's name, Commercial and Government Entity (CAGE) Code (if available), level of facility clearance (if available), address, primary point of contact, business size, and status of U.S. ownership.

Respondents shall also identify the applicable 10 U.S.C. § 2371b eligibility criteria related to the response (*please identify only one*):

- There is at least one nontraditional defense contractor (*defined below*) or nonprofit research institution participating to a significant extent in the project**; OR**

- All significant participants in the transaction other than the Federal Government are small businesses (including small businesses participating in a program described under section 9 of the Small Business Act (15 U.S.C. § 638)) or nontraditional defense contractors**; OR**

- At least one third of the total cost of the project is to be provided by sources other than the Federal Government.

Note: A *Nontraditional Defense Contractor* is defined as an entity that is not currently performing and has not performed, for at least the one-year period preceding the solicitation of sources by the Department of Defense (DOD) for the procurement of transaction, any contract or subcontract for the DOD that is subject to full coverage under the cost accounting standards prescribed pursuant to 41 U.S.Code § 1502 and the regulations implementing such section.

ii. Technical Response:

Responses should be constructed to align with the order of the instructions below (1 - 8).

1. Solution Narrative: Respondents shall describe the approach used to design/deliver a unique Phase 1 prototype solution for the prototype technology objectives defined in RFS Section 5, Desired End-State Objective(s), to include any attachments. While these focus areas are of significant importance, responses will be considered as a whole. No pricing shall be included in the technical response.

   The Solution Narrative must also include a discussion on schedule and the timing of all deliverable(s) to include those outlined within RFS Section 6, Project Deliverables.

2. Explanation Supporting Eligibility for Award of a Prototype OTA:

   Respondents shall provide rationale to support the specific condition that permits award of an OTA to the proposed prime contractor/performer. The onus of proof to support *nontraditional participation to a significant extent; small business or nontraditional defense contractor status;* or any *cost sharing arrangement* lies with the respondent and has a direct correlation to award eligibility.

3. Foreign Owned, Controlled, or Influenced (FOCI) Documentation (if applicable): Documentation may include, but is not limited to: Standard Form 328 (Certificate Pertaining to Foreign Interest); Listing of Key Management Personnel; an Organizational Chart; Security Control Agreements: Special Security Agreements; and Proxy Agreements or Voting Trust Agreements. It is recommended companies who fall within the FOCI category visit https://www.dss.mil for additional guidance and instruction.

4. Government Furnished Property or Information: Respondents must clearly identify if its proposed solution depends on Government Furnished Information (GFI) / Government Furnished Property (GFP) or other forms of Government support (i.e. laboratory or facility access), etc.

   If so, the response must specify the GFI/GFP required. Respondents must clearly identify if its proposed solution depends on GFI/GFP or other forms of Government support be provided, the impact to the solution if the requested information/property/asset is not available, and will confirm the details with the respondent prior to any proposal revisions or selection, if applicable.

5. Mandatory Compliance with Restrictions: Respondents must address the restrictions identified within RFS Section 8, Security Classification, Respondent Restrictions, and other Required Compliance, and explain how each regulation or standard is currently, or will be met.

6. Task Description Document (Not Included Within Page Count): Respondents must provide a Task Description Document (TDD) outlining the project tasks to be performed along with schedule milestones and delivery dates required for successful completion. It is anticipated that, if selected, the proposed TDD will be incorporated into the resultant OTA. Respondents are encouraged to be concise but

thorough when outlining their work statements. The TDD may be submitted as an appendix or a separate file as part of the proposal.

7. Summary of Subcontractor Participation (if applicable): Respondents must identify all subcontractors involved and their role within the performance of the proposed concept. The information must include the following:

    a. Subcontractor company name, Commercial and Government Entity (CAGE) Code (if available), level of facility clearance (if available), address, primary point of contact, business size, and status of U.S. ownership.

    b. If the subcontracted company's involvement is considered significant, rationale supporting the significance must be present within the narrative. The onus of proof to support participation to a significant extent or any cost sharing arrangement lies with the respondent and has a direct correlation to award eligibility.

    c. If applicable, Foreign Owned, Controlled, or Influenced (FOCI) Mitigation Documentation shall be provided for subcontractors and will not count towards the page count.

8. Data Rights Assertions and Level of Rights Proposed:

    a. The rights offered should be displayed in a manner that allows for ease of discussion in determining trade-offs and potential options for long-term sustainability of the deliverables of this effort.

    b. If rights are being asserted at a level less than the Government's desired level of allocation (see RFS Section 9, Level of Data Rights Requested by the Government), respondents must provide detail explaining the specific rationale for the assertion. Please also review 10(b)(iii)(5) below for additional requirements related to data rights pricing.

    c. Any items previously developed with federal funding (and used for the proposed solution) should clearly identify all individual components funded by the Government and the recipient of the deliverables.

    d. If commercial software is proposed as part of the prototype solution, all applicable software licenses must be identified and included with the response. Note that any software license term or condition inconsistent with federal law will be negotiated out of the license.

iii. Price Response:

The price response shall be submitted as a separate file from the technical response. No pricing details shall be included in the technical response. This project will employ the following pricing structure:

☒ Fixed Price with Payable Milestones
☐ Expenditure Basis (cost reimbursable)

1. The overall total price should be divided among severable increments that align to a proposed milestone payment schedule. Milestones are not required to match actual expenditures but should realistically align to the effort expended or products delivered.

2. In order to support the Government's evaluation of fair and reasonable pricing, the respondent shall delineate the key pricing components, and show clear traceability to the sub-phases, the individual tasks within each sub-phase, and/or milestones of the Technical Response. At a minimum, key pricing components include Labor Total(s), Other Direct Costs/Material Total(s), License prices and Subcontractor price(s). Data should be segregated by each key objective, milestone, and/or phase proposed.

3. Include a brief narrative that explains your pricing structure and maps the proposed prices to the solution's technical approach.

4. Including a Basis of Estimate to support your pricing may substantially expedite evaluation of your response.

5. If limited or restricted rights are being asserted within the response, a table that includes prices for both Government Purpose Rights and Unlimited Rights for any limited or restricted item must be included.

6. Any additional features or capabilities that extend beyond the currently requested core technical objectives shall be separately priced for the Government's consideration. Pending funding availability and need, the Government may fund these advanced features at a later date.

11. Evaluation Process and Methodology:

a. Individual responses will be evaluated with consideration given to:
   i. Demonstrated expertise and overall technical merit of the response;
   ii. Feasibility of implementation; and
   iii. Total project risk as it relates to the technical focus areas, price and schedule

b. The Government will evaluate the degree to which the proposed solution provides a thorough, flexible, and sound approach in response to the prototype technical objectives

as stated in RFS Section 5, Desired End-State Objectives, as well as the ability to fulfill the objectives in this RFS.

c. The Government will award this project, via S^2MARTS (Agreement No. N00164-19-9-0001), to the respondent(s) whose solution is assessed to be the most advantageous to the Government, when price, schedule, technical risks, the level of data rights, and other factors are considered. The Government reserves the right to award to a respondent that does not meet all the requirements of the RFS.

d. The proposed project price, schedule, and intellectual property/data rights assertions will be considered as aspects of the entire response when weighing risk and reward. The assessment of risks is subjective and will consider all aspects of the proposed solution. Respondents are responsible for identifying risks within their submissions, as well as providing specific mitigating solutions.

e. The Government reserves the right to reject a submission and deem it ineligible for consideration if the response is incomplete and/or does not clearly provide the requested information. Debriefings will not be provided.

12. Follow-On Activity:

a. Upon successful completion of this prototype effort, the Government anticipates that a follow-on production effort may be awarded via either contract or transaction, without the use of competitive procedures if the participants in this transaction successfully complete the prototype project as competitively awarded from this document. The prototype effort will be considered successfully complete upon demonstration of the aforementioned technology objectives.

b. Successful completion for a specific capability may occur prior to the conclusion of the project to allow the Government to transition that aspect of the prototype project into production while other aspects of the prototype project have yet to be completed.

c. Requirements of other potential follow-on activities could involve, though not limited to, continued development and baseline management, fielding, sustainment, training, further scaling of the solution, integration of future capabilities, or integration of the solution with other capabilities.

13. Attachments

a. Section 889 Prohibition and Reporting

b. Section 889 Verification and Representation

c. DD254 – Contract Security Classification Specification

14. Important Dates

a. Questions related to this RFS shall be submitted no later than Thursday, January 28, 2021.

   To submit any questions, visit the opportunities page at www.nstxl.org/opportunities, select the "Current" tab, locate the respective project, and select "Submit a Question".

b. Proposals submitted in response to this RFS are due no later than Monday, February 15, 2021.

c. To submit your proposal, visit the opportunities page at www.nstxl.org/opportunities, select the "Current" tab, locate the respective project, and select the "Submit Proposal" link. You must have an active account and be logged-in to submit your response.

d. RFS Respondents must be active members of the consortium at the time of proposal submission.

15. Additional Project Information

a. The Government intends to award one Other Transaction Agreement as a result of this RFS; however, more than one award may be made if determined to be in the Government's best interest. The Government also reserves the right to not select any of the solutions proposed.

b. Acceptable responses not selected for the immediate award will be retained by NSTXL & the Government for possible future execution and funding. The non-selected proposals will be considered as viable alternatives for up to 36 months. If a proposal (that was not previously selected) is determined to be a suitable alternative, the company will be contacted to discuss any proposal updates and details of a subsequent project award.

   Respondents whose proposals are not selected for the initial award shall not contact the Government or NSTXL to inquire about the status of any ongoing effort as it relates to the likelihood of their company being selected as a future alternative.

c. The United States Navy, specifically Naval Surface Warfare Center, Crane Division, has release authority on any publications related to this prototype project.

d. Unsuccessful respondents will be notified, however, debriefings for this project are not required nor planned at this time.

e. If resource-sharing is proposed in accordance with 10 U.S. Code § 2371b(d)(1)(C), then the non-Federal amounts counted as provided, or to be provided, by parties other than the Federal Government may not include costs that were incurred before the date on which the OT agreement becomes effective. Costs offered as a resource-share that

were incurred for a project after the beginning of negotiations, but prior to the date the OT agreement becomes effective, may be counted as non-Federal amounts if and to the extent that the Agreements Officer determines in writing that: (1) the party other than the Federal Government incurred the costs in anticipation of the OT agreement; and (2) it was appropriate for the entity to incur the costs before the OT agreement became effective in order to ensure the successful implementation of the OT agreement.

f. Certain types of information submitted to the Department during the RFS and award process of an OT are exempt from disclosure requirements of 5 U.S.C. §552 (the Freedom of Information Act or FOIA) for a period of five years from the date the Department receives the information. It is recommended that respondents mark business plans and technical information that are to be protected for five years from FOIA disclosure with a legend identifying the documents as being submitted on a business confidential basis.

g. No classified data shall be submitted within the proposal. To the extent that the project involves DoD controlled unclassified information, respondents must comply with DoDI 8582.01 and DoDM 5200.01 Volume 4. Respondents must implement the security requirements in NIST SP 800-171 for safeguarding the unclassified internal information system; and must report any cyber incidents that affect the controlled unclassified information directly to DoD at https://dibnet.dod.mil.

h. Export controls: Research findings and technology developments arising from the resulting proposed solution may constitute a significant enhancement to the national defense and to the economic vitality of the United States. As such, in the conduct of all work related to this effort, the selected performer must comply strictly with the International Traffic in Arms Regulation (22 C.F.R. §§ 120-130), the National Industrial Security Program Operating Manual (DoD 5220.22-M) and the Department of Commerce Export Regulation (15 C.F.R. §§ 730-774).