S²MARTS Project: Co-Packaged Analog-Drive High-Bandwidth Optical Input/Output (KANAGAWA)
Request For Solutions (RFS) Question & Answer | Date: July 8, 2022

1. Question: **With regards to the CPOs, are we supposed to also leverage internal technology (VCSEL) or are you looking for packaging technology?**

Answer: KANAGAWA is open to any laser solution that enables the fiber links between chiplets within the efficiency goal of 5 pJ/bit.

2. Question: **Is the CPO limited to transmitter/detectors and corresponding TIA/drivers and controls are external, or is this optional?**

Answer: Task A deliverables should include all necessary electronic control and signal conditioning circuits such that they can be directly driven by existing SerDes. Proposers that disaggregate optical and electronic functions on multiple chips should disclose any package-level considerations required by their approach within proposals.

3. Question: **Is there a reason for a 2Tb/s limit and is this limited by the data rate and number of lanes?**

Answer: KANAGAWA does not require a specific number of lanes or per-lane data rate. Aggregate bandwidth must reach at least 2 Tbps in Iteration 2, and concepts that exceed this goal are welcomed.

4. Question: **How will IP be protected?**

Answer: During proposal evaluation: Proposals will be reviewed by a cross service team of USG reviewers. By law government employees are bound to protect the IP disclosed in the proposals. Additionally, the evaluation team is required to complete additional processes, including, but not limited to ethics training regarding conflict of interest, and non-disclosure agreements.

During the project: the performers will be responsible for standing up the appropriate legal protections (e.g., NDAs) between one another at the beginning of the program.

5. Question: **Unpriced option, page 8 – Thermal Control System – is that for Task A or Task B performer?**

Answer: See Question 49 for more details on the nature of Unpriced Options. Depending on the trajectory of the program, Task A and/or Task B performers could potentially solicited for unpriced option proposals supporting a thermal control system.

6. Question: **What technical data is expected to be shared amongst the 2– 3 Task B performers? Would there be a contractual mechanism in place to ensure Task A performer does not share one Task B performer information with another Task B performer?**

Answer: The performers will be responsible for standing up the appropriate legal protections (e.g., NDAs) between one another at the beginning of the program.

7. Question: **Is the Task A performer responsible for providing the Electrical Die and/or package BOM items (interposer, lid, etc) for the Task B CPO/MCP assembly?**

Answer: No.

8. Question: **Who is responsible for designing the CPO / MCP assembly? This would include design of the package (interposer, lid, BGA I/O assignment), and digital design (overall functionality, correct I/O mapping and signal integrity between the Silicon Photonics and Electrical Die).**

Answer: Task B performers are responsible for this activity.

9. Question: **Reliability - For B-1.04 Proxy Integration experiments - Are there any specific reliability and environmental assessments that the government wants/recommends to be included (aside from shock and vibe which is listed)? Due to short time line in B-1, is reliability performance testing using the proxy assembly expected as part of B-1.04? Given proxy die will be received by Month 3, and assuming another couple months for assembly, it will be challenging to collect environmental testing data in Phase 1.**

Answer: Task B Phase 1 includes a reliability and environmental assessment, but the KANAGAWA RFS does not require any specific environmental testing in Phase 1. It is acceptable for the assessment to consist of modeling that is informed by data obtained from the heterogeneous integration experiments.

10. Question: **Since the sample size provided by Task A performer is relative small, to make statistically meaningful conclusions on reliability, can USG clarify on reliability and environmental measurement expectations?**

Answer: The goal of the Task B environmental measurements is to demonstrate operation in representative environments and to characterize performance under varying conditions. High-fidelity statistics are not required.

11. Question: **What are the known failure mechanisms aside from mechanical integrity that have been observed?**

Answer: Proposers may identify any expected failure mechanisms for their approach.

12. Question: **What is the official NSWC Crane Division address and CODE to be used on Project KANAGAWA related forms (e.g., Certs & Reps forms)?**

Answer: Naval Surface Warfare Center, Crane Division, Code 024
300 Highway 361, Crane, IN 47522

13. Question: **Regarding the 5pg limit on the Price Proposal for Gray Summer, is this a combined total if there are subcontractors, or is each institution given 5 pg max?**

Answer: Not applicable; these responses concern the KANAGAWA project, not the Gray Summer project.

14. Question: **When are the expected awards, and when does the schedule start?**

Answer: Notionally, assume an Oct 1 award with a Nov 1 kickoff.

15. Question: **How much time is allocated to contract review and finalization before the schedule start?**

Answer: Notionally, assume an Oct 1 award with a Nov 1 kickoff.

16. Question: **For the unpriced options, are we just to respond that we can support the request, or what is required?**

Answer: Merely acknowledgement by the applicant is sufficient. In order to ensure maximum competition, we are publically disclosing that these options prior to award of the base contract.

17. Question: Task B - When will the electrical interfaces be defined?

Answer: Task B performers should define their electrical interface within Phase 1.

18. Question: When will negotiations commence for task B2/B3?

Answer: The USG can choose to initiate "Conversations" with any given applicant. If selected for "Conversations," it is notionally expected that those conversations could occur Aug 12-26.

19. Question: Are you able to disclose who the technical evaluators are going to be?

Answer: No.

20. Question: In the live talk presentation, a lot of the material presented was from AYAR Labs, will they be an evaluator?

Answer: No. Only USG employees or "government-like" contractors (e.g., DARPA SETAs) with appropriate legal IP protections (e.g., NDAs, COI forms/training, etc.) will participate in the evaluation of proposals. Only USG employees will retain voting privileges for recommending awardees.

21. Question: How will IP be protected as part of the BID documentation in the instance of not being selected?

Answer: See Section G of the RFS.

22. Question: Please confirm if the operational temperature requirement of -55ºC to 125ºC corresponds to the device junction temperature, the chiplet temperature or the packaged ambient temperature?

Answer: Package ambient temperature.

23. Question: Are there going to be any requirements with regards to VITA or SOSA?

Answer: No.

24. Question: NSTXL requires that participants are US Based, so if we use secondary suppliers that are based in Japan/Canada, but have manufacturing capability in the US, is that acceptable?

Answer: See Section C of the RFS. It is acceptable that that non-US companies apply to KANAGAWA. Companies that have a path towards Trusted and/or Assured partnership with the USG will be preferred during the selection process. Although domestic/trusted manufacturing is a clear preference for the USG, it is not within the funding scope of this program to redirect supplemental supply chains.

25. Question: For post award, is the minimum requirement for project work "US Person" or can people with VISAs from NATO/5EYES countries work on the project?

Answer: No explicit language is included in the RFS regarding this topic. Applicants are expected to be able to handle controlled unclassified information and comply with ITAR regulations.

26. Question: **Is there a data rate limit on what can be proposed?**

Answer: KANAGAWA does not require a specific number of channels or per-channel data rate. Aggregate bandwidth must reach at least 2 Tbps in Iteration 2, and concepts that exceed this goal are welcomed.

27. Question: **Are the devices supposed to support multi-rate solutions (for example 1G to 10G or 25G to 100G)?**

Answer: KANAGAWA does not require multi-rate solutions, but they may be advantageous to enabling multiple MCP configurations.

28. Question: **Is there a modulation format that has to be adhered to (NRZ, PAM4, etc)?**

Answer: No.

29. Question: **Is the technology limited to fixed wavelength, or is tunable of interest?**

Answer: The RFS does not specify an operating wavelength or WDM grid. While O band and C band are common choices in the industry, proposers may choose wavelengths to support their particular fiber link solution.

30. Question: **Is the proposal limited to wavelengths in the O-Band or are other WDM bands options (E, S, C, L)?**

Answer: The RFS does not specify an operating wavelength or WDM grid. While O band and C band are common choices in the industry, proposers may choose wavelengths to support their particular fiber link solution.

31. Question: **Are there any reference standards that need to be followed, such as LAN-WDM, CW-WDM, CWDM, etc?**

Answer: No. However, please note in the proposal if a specific standard is targeted by a proposal.

32. Question: **What is the minimum wavelength spacing required?**

Answer: Task B performers should define their electrical interface within Phase 1.

33. Question: **Is there going to be a minimum interoperability requirement set by the OUSD (R&E) Trusted & Assured Microelectronics?**

Answer: No.

34. Question: **Is there a defined electrical interface requirement between the packaged chiplet and the FPGA?**

Answer: Task B performers should define their electrical interface within Phase 1.

35. Question: **Is the Co-Packaged Analog-Drive High-Bandwidth Optical Input/Output chiplet a configuration of the driver-laser-mux/demux-detector-TIA, and or can it include anything else?**

Answer: Task A deliverables should include all necessary electronic control and signal conditioning circuits such that they can be directly driven by existing SERDES. Proposers that disaggregate optical and electronic functions on multiple chips should disclose any package-level considerations required by their approach within proposals.

36. Question: If considering PAM4, will the FPGA drive PAM4 or will this need to be managed at the chiplet level?

Answer: Task A deliverables should include all necessary electronic control and signal conditioning circuits such that they can be directly driven by existing SERDES. Proposers that disaggregate optical and electronic functions on multiple chips should disclose any package-level considerations required by their approach within proposals.

37. Question: Can you confirm that the SERDES will be covered by a third party, and that the SERDES will or will not have a CDR?

Answer: It is expected that SERDES will be included in third party chip designs that are identified and procured by Task B performers for MCP development.

38. Question: Will there be a requirements with regards to MCM, and will the ICs (FPGA/MCU/ASIC) be required to be part of the solution or is the exercise purely about packaging the chiplet? If yes, will NSWC Crane be providing which chips need to be used and will this be provided in B1 or at a later phase B2/B3 or an unpriced option?

Answer: It is expected that SERDES will be included in third party chip designs that are identified and procured by Task B performers for MCP development.

39. Question: Regarding the environmental characterization for the temperature range of -55 to 125C and the statement, "It is expected that meeting these conditions will entail a thermal control system, particularly for lasers. Proposals should discuss the expected methods of thermal control and corresponding size, weight, and power considerations." Is the power of the thermal control system expected to be included in the chiplet energy efficiency of 5pJ/bit?

Answer: No.

40. Question: Is the chiplet required to operate at <5pJ/bit energy efficiency continuously and without interruption over the full temperature range of -55 to 125C?

Answer: No, it is acceptable for different versions of components, particularly lasers, to address portions of the full temperature range.

41. Question: Regarding the anticipated CUI technology for the Program, can you please provide the Security Classification Guide as required by DoDM 5200.01 or a similar level of information clarifying the precise elements of information and technology to be classified as CUI so that participants can properly address in their proposals?

Answer: The intent of the cited requirement is to ensure that Classified data does not find its way into a CUI proposal. With this in mind, it is the responsibility of each applicant to identify and disclose relevant Security Classification Guides (SCGs) associated with their proposed technology and applications. If proposing a secure process for Task B, it may be relevant to perform such a study in Task B-1.

42. Question: Is the electro-optical transceiver allowed to reset if it has to switch from one temperature range to another? If yes, what is the allowed transition time?"

Answer: Yes. The RFS does not specify a transition time.

43. Question: I have a technology to additively manufacturing Silicon Carbide for a polymer precursor and directly interface it with an additively manufactured metal structure. Would that concept be valid for this program. I just picked up an Air Force Phase II STTR on the concept.

Answer: The concept does not appear relevant based on the brief description, but KANAGAWA is open to any approach that meets RFS goals, metrics, and deliverables.

44. Question: What is the considered, "installed depreciable life" expectancy?

Answer: This is term is tied to the lifetime denoted in the applicant's financial books.

45. Question: What if any requirements exist around the manufacturing location of the solution? Is there a requirement for all products manufacturing to be "Made in the USA".

Answer: See Question 24.

46. Question: Is there a specific Link-Budget metric as defined by the application usage?

Answer: No.

47. Question: Are there any preferred physical layout constraints between the laser and the optical silicon? Are there any preferred physical co-location requirements between the Laser and Chiplet device? (I.e.Does the expected end use case enable the laser and chiplet to be co-located on an identical board, could the Laser be disaggregated from the chiplet device, if so what is the use case inter device distance requirement)?

Answer: The laser may be external to the chiplet and MCP. The KANAGAWA RFS does not specify a distance requirement between laser and chiplet components.

48. Question: Are all MIL-SPEC temperature metrics of success in Task A2 weighted the same?" Could there be different solutions for different operating temperature ranges? (i.e. a solution for very cold -55C to 0C, Medium 0C to 80C High 80C to 125C, temperature ranges listed are notional)? Could there be different or separate product solutions for each temperature range? Or is one MCP required to cover the MIL-SPEC temperature range in its entirety?

Answer: It is acceptable for different versions of components, particularly lasers, to address portions of the full temperature range.

49. Question: When, and How will the "Unpriced Options" be evaluated? Can we submit "unpriced options" with the initial submission? Is there a ROM budget for these unpriced options? Are the unpriced options a paper study or is there a technical demonstration required.

Answer: Unpriced options should be submitted if and only if they have been requested by the USG, and will only come after the time of award. More information (such as technical requirements and financial ROMs) will be provided at the time of request. Given the nature of the program, it highly likely that many of the options could require technical demonstration.

50. Question: **Please confirm that the energy efficiency (5pJ/b) and latency (4ns+TOF) targets refer only to the optical chiplet and link, and does not include any SERDES latency or power in the host dies.**

Answer: This is correct.

51. Question: **For serial-in electrical interface implementation in KANAGAWA, is there an expectation of edge BW density match between standard FPGA die and optical chiplet? Is there a maximum mismatch allowed?**

Answer: KANAGAWA does not specify an edge bandwidth density requirement.

52. Question: **Is there target for product of edge BW density and Energy Efficiency for KANAGAWA (Gbps/mm)/ (pJ/bit)?**

Answer: KANAGAWA does not specify an edge bandwidth density requirement.

53. Question: **Can you please help clarify the entry criteria for Task B? It only says 2.5D capability and path to product? Does that include just a proposal along with proof of OSAT partnership?**

Answer: The primary goal of KANAGAWA is to ensure maximize the proliferation of optical I/O chiplets and lasers by inserting them into production-level manufacturing facilities which have a path towards Trust certification and application of the Microelectronics Assurance Framework. Therefore, proposals authored by Defense Industrial Base players with known production-level 2.5D integration will be prioritized. To be clear, university-based foundries/packaging facilities are not considered a priority interest for this investment. Applicants for Task B may increase competitiveness of their proposal by identifying the existing MRL, volume, partners/customers, and trusted status associated with their company's existing advanced packaging capabilities. The more experience a company has demonstrated in these areas, the more risk will be burned down for KANAGAWA.

54. Question: **Can you please clarify the full form of SDP (System Demonstration Platform)?**

Answer: For the intent of this RFS, the acronym "SDP" stands for "single-die package."

55. Question: **V groove qualification: Is there a hard constraint on V grooves? Or are other coupling schemes acceptable?**

Answer: Other coupling schemes are acceptable provided that they address the specified performance and MRL criteria.

56. Question: **Chiplet Yield : In case of Heterogeneous architecture would be assembly/ Engine yield. Please confirm**

Answer: The KANAGAWA chiplet yield requirement refers to functional test of I/O control circuitry.

57. Question: **Does the latency of 4ns and BER of 10^-12 include the SerDes ? This would help define understand if latency requirements is pre-FEC**

Answer: No.

58. Question: **Is there a BW density (Tbps/mm) requirement?**

Answer: No.

59. Question: Does the 5pJ/bit include SerDes power as well? If yes, is the expectation to demonstrate the end to end link including SerDes Chip?

Answer: No.

60. Question: Please confirm that Optical I/O Chiplet is defined at transceiver level. In other words, Optical I/O Chiplet include both PMD IC (driver+TIA) + PIC if we consider a heterogeneous architecture. So, the expectation would be to produce 50 PIC+ PMD IC Engine assemblies when there is a request for 50 Optical I/O dies. Please confirm that my understanding is accurate. If yes, would separate sets of EIC dies and PIC dies be acceptable for entry criteria as long as architecture looks good?

Answer: Task A deliverables should include all necessary electronic control and signal conditioning circuits such that they can be directly driven by existing SERDES. Proposers that disaggregate optical and electronic functions on multiple chips should disclose any package-level considerations required by their approach within proposals.

61. Question: What would the USG consider a useful starting point for early independent verification and validation (IV&V) engagement with a Task A performer?

Answer: The USG would be interested in the delivery of demonstration boards/setups (for both lasers and optical I/O die) currently offered by the Task A company. Please feel free to include in the cost proposal. Though not guaranteed, there may be a potential to discuss in “Conversations” after solution submission.