S²MARTS Project 20-06: Rapid Assured Microelectronics Prototypes using Advanced Commercial Capabilities

(RAMP) Phase 2

Request For Design (RFD) Questions & Answers | Posted February 23, 2021

1. **Question**: As experts in directly relevant areas that have done a lot of work in the TSMC 16nm and the GF 12nm processes, we are wondering if you have selected one of these processes or something similar. In case you are not using one of those processes, an advantage of our technology is the ability to quickly transfer our library and circuits to another process at a significant cost savings. Is this something that would benefit your program?

   Response: a) The RAMP Phase 2 demonstration designs are focused on using an on-shore foundries (Intel 22 FFL or GlobalFoundries 12LP). b) Any technology to transfer existing designs from different technology nodes would have to be evaluated if designs were selected for RAMP.

2. **Question**: What IP (if any) will provided for designers to use - either for IBM-lead, or Microsoft-lead - and for GF 12LP and Intel 22FFL?

   Response: No IP will be provided. All required third party or special IP should be included in the RFD ROM and with the Phase 2 RAMP Performer Contract.

3. **Question**: What EDA tools will provided for designers to use - either for IBM-lead, or Microsoft-lead - and for GF 12LP and Intel 22FFL?

   Response: Standard EDA tools will be provided by the Phase 2 RAMP performer using the RAMP platform. Any other EDA tools that are required should be listed in the proposal and included in the ROM.

4. **Question**: How can a DIB provide sensitive details (e.g. classified) to the Government – that require secure channels?

   Response: No classified designs will be selected for RAMP Phase 2 proto-type demonstration designs.

5. **Question**: Is the chiplet a small accelerator?

   Response: The chiplet function is not specified. The design should further enable DoD specific applications in a multi-chip package.

6. **Question**: Clarify front-end design complete within 60 days: does it mean frozen netlist?

Response: Yes, a frozen netlist is needed to start on back-end design process.

7. **Question**: Can you clarify what is 3rd Party DoD IP? Will this be made available to performers?

   Response: a) Third party DoD IP is referring IP that is developed by a DIB for use in a DoD system. b) No

8. **Question**: Do we include packaging in our ROM?

   Response: If the design selected is a chiplet, then package and testing can be coordinated using the SHIP program. If the design is not a chiplet, the design performer should coordinate package and testing with the RAMP Phase 2 performer. Note, SHIP includes Intel (high-end MCP), Qorvo (RF and more traditional packaging) and a yet to be announced digital packaging performer.

9. **Question**: Will ATPG be tested at foundry?

   Response: There are no current plans to test ATPG at the foundry. Any foundry testing will be coordinated with RAMP Phase 2 performer.

10. **Question**: Who is responsible for wafer and package testing? If Intel, then will wafer and package testing be in an ITAR facilitate?

    Response: a) The RAMP Phase 2 performer will coordinate with selected design proposer for wafer and package testing. b) If the design selected is a chiplet, then package and testing will be coordinated using the SHIP program. If the design is not a chiplet, the design performer should coordinate package and testing with the RAMP Phase 2 performer. Note, SHIP includes Intel (high-end MCP), Qorvo (RF and more traditional packaging) and a yet to be announced digital packaging performer.

11. **Question**: Is this a dedicated run or MPW? Who owns the masks?

    Response: a) If available, the goal is to use T&AM funded MPW runs for the three RAMP Phase 2 demonstration designs. b) The government controls the use of the masks

12. **Question**: Who owns the MPW? Can we get more DIE beyond the few prototype versions?

    Response: a) The government controls the MPW run b) For DMEA/GF, the typically die allotment is 100 die per rider. Additional die may be available depending on the dicing plan and reticle plan.
    For MOSIS/Intel, the die allotment is 100 die per rider.
    Additional wafers can be purchased, and will be considered based on the justification for additional die.

13. **Question**: Does 10 page White Paper limit include cover sheet/front matter?

    Response: Yes

14. **Question**: Do we include tapeout cost in our ROM?

    Response: No, if possible, the goal is to use T&AM funded MPW runs for the three RAMP Phase 2 demonstration designs. The RAMP Phase 2 performer will include optional Phase 2 MPW cost in their

Phase 2 proposals. This will support the case if the T&AM MPW is not available or does not align with RAMP Phase 2 design schedules.

15. **Question**: Please clarify the information being requested for Input/Output Signal List.

    Response: The Standard Pin List with description for the proposed design.

16. **Question**: Is the RAMP chiplet intended to be the same as the SHIP-Digital chiplet POC?

    Response: Designs that were proposed to the SHIP Chiplet RFD can be submitted to this request, however, designs that were not aligned with the SHIP Digital chiplet objectives are being sought as well.

17. **Question**: When is the RAMP tapeout date?

    Response: The tape-out date depends on the following:
    a) Complexity of the design selected for the RAMP
    b) How long it take to do the do the front-end and back-end portions of the design.

    The period of performance for RAMP Phase 2 is 18 months, so the goal is have design, fabrication, packaging and testing completed during that period.

18. **Question**: What type of contract is Phase II expected to be issued as? FFP? CPFF?

    Response: Will be determined at award. Firm Fixed price is preferred.

19. **Question**: Are attachments counted in the 10 page white paper limit?

    Response: No

20. **Question**: Is quantitative assurance technology required for all the design categories?

    Response: Yes

21. **Question**: Are there any quantitative assurance requirements?

    Response: The design performer will work the RAMP Phase 2 performer to meet the quantitative assurance requirements during design and fabrication.

22. **Question**: Will the tools employed through the RAMP sponsors be provided to the proposers, or are they operated solely by the RAMP awardees?

    Response: EDA tools will be available on the RAMP platform and provided by the RAMP Phase 2 performer. EDA required tools not on the RAMP platform would have to included on RAMP Phase 2 Performers ROM.

23. **Question**: Will the proposer be responsible for the entire physical design, with the RAMP awardees providing an oversight or secure fabrication flow?

Response: The demonstration ICs will be designed by the DIB and will span a wide range of physical design support models from support-only to turnkey physical design by the design capability. The design proposer will identify their preferred approach on the RAMP-2 RFD Response Worksheet, question 7.

24. Question: Will circuit IP be provided by the program or will performers need to price this?

Response: The performer will need to price circuit IP. There will be no IP provided by the government.

25. Question: The SHIP SOO shows a 15 July 2021 tape-In date. Will fabrication on the RAMP Phase 2 program target the same tape-in date?

Response: No, that is independent of RAMP.

26. Question: Specifics of cost may depend on which of the Phase 1 primes advances to Phase 2. Is there guidance on how this aspect of the proposed effort should be priced?

Response: Design cost should not include items provided by the RAMP Phase 2 performers like their design support, EDA tool costs, RAMP platform. They will provide those costs in there RAMP Phase 2 ROMs. The ROM for this RFD is intended to cover the design proposer's management/engineering time, IP cost, packaging/testing (if not SHIP). It is preferred to break out the ROM in categories to identify cost for each area. The intent is to have a ROM when evaluating the designs. The final ROM will be included in the RAMP Phase 2 performer's ROM.

27. Question: TSMC 16nm and the GF 12nm processes – has the Government selected one of these processes or something similar for the RAMP approach already?

Response: The RAMP Phase 2 goal is to use Intel 22 FFL or GlobalFoundries 12LP.