STRATEGIC & SPECTRUM MISSIONS ADVANCED RESILIENT TRUSTED SYSTEMS (S^{2}MARTS)
REQUEST FOR DESIGNS (RFD)

in support of the

Rapid Assured Microelectronics Prototypes using Advanced Commercial Capabilities (RAMP) Phase 2

PROTOTYPE PROJECT REQUEST FOR DESIGNS

Project No. 20-06

This request for information is open to the public and not restricted to members of the NSTXL consortium. This is not a funded opportunity for award.

1. **Project Title:** Rapid Assured Microelectronics Prototypes using Advanced Commercial Capabilities (RAMP) Phase 2 – Request For Design

2. **Prototype Project Sponsor/Requiring Activity:** Naval Surface Warfare Center, Crane Division, Trusted Microelectronics Division (GXV)

3. **Contracting Activity:** Naval Surface Warfare Center, Crane Division, Code 0221

4. **RAMP Phase 2 Design:** This Request for Designs (RFD) is to evaluate potential DoD relevant designs that can be implemented during Phase 2 of the ongoing RAMP program.

   As a result of this announcement, it is the Government's intention to review & select three potential designs from the US Defense Industrial Base (DIB) targeting DoD specific applications. Upon selection of a viable design the Government intends to subsequently assist with transitioning the selected company/ies onto an active performer's team over the course of Phase 2 implementation of the RAMP program.

   RAMP Phase 2 will demonstrate the implementation of the capabilities developed in Phase 1 by exercising the design, fabrication, and test of at least three DoD relevant designs. At least one design shall be a System On a Chip (SOC) that incorporates commercial and DoD application specific Intellectual Property (IP), one shall be a mixed-signal IC, and one may be a chiplet design. The demonstrated integrated circuits (IC) should be designed by the Defense Industrial Base (DIB) and can span a wide range of physical design support models from support-only to turnkey physical design by the design capability.

5. RAMP Background:

Description: The Rapid Assured Microelectronic Prototypes Using Advanced Commercial Capabilities (RAMP) prototype project addresses brand new technology development that will provide DoD relevant IC prototypes utilizing advanced node fabrication that mitigate the need for International Traffic in Arms Regulations (ITAR) fabrication. The goal of RAMP is the establishment of a Secure Design Capability that supports an enhanced physical design by the DIB in state-of-the-art (SOTA, defined as ≤ 22nm node Si CMOS) technology nodes. The secure design process will apply methods to ensure both the confidentiality and integrity of circuits during the design and fabrication flow. A key part of this is the establishment of assurance data to provide a quantitative evaluation of the supply chain.

The Phase I (6 months) objective will be achieved through three major tasks (4QFY20 – FY21)

1. Establishment of Secure Design Capability that supports an enhanced physical design by the DIB in SOTA (defined as ≤ 22nm node Si CMOS) technology nodes.
2. Application of methods to ensure both the confidentiality and integrity of circuits during the manufacturing/fabrication flow.
3. Definition of a DoD supply chain standard that leverages commercial microelectronics supply chain security methods to meet DoD needs.

Phase 2: (18 Months), FY21-FY22

1. Tasks 1 & 2: Demonstrate secure design capability and quantifiable assurance technology to design and build DoD relevant designs with the DIB.
2. Task 3: Demonstration of implementation prototype standards in at least one dual-use integrated circuit and one custom DoD integrated circuit.

Currently IBM and Microsoft are RAMP Phase 1 performers.

6. RAMP Phase 2 Design Schedule:

Milestones	**Date**
Release of Request for Designs - RAMP Phase 2	January 2021
Deadline for RAMP Phase 2 designs	February 2021
RAMP Phase 2 design selections complete	March 2021
RAMP Phase I – end of Period of Performance	April 30 2021
RAMP Phase 2 Period of Performance	May 2021 to November 2022

RAMP Phase 2 DIB Front-end Design Implementation	May 2021 to July 2021
RAMP Phase 2 DIB Back-end Design Implementation, fabrication, packaging and test.	July 2021 to November 2022

7. Design Parameters

The design parameters listed below are guidelines and are not intended to preclude designs from being submitted or selected. The goal is to select a mature design (< 60 days of front-end design work needed to complete at the beginning of Phase 2). The DIB design team will work with the RAMP Performer for Quantifiable Assurance (QA), supply chain, design environment and design transfer. The Government is interested in selecting one Chiplet design that uses the packaging and interface technology developed in the State-of-the-Art Heterogeneous Integration Prototype (SHIP) program.

SoC Chip:

1. > 25M gates (NAND2 Equivalent) w/o memory
2. > 20Mb of SRAM (Static Access Random Memory)
3. At least one controlling processing unit
4. At least one high speed SERDES (Serializer/Deserializer) IO (Input Output) operating above 12 Gb/sec
5. At least two additional processors/accelerators
6. Clock speed > 1GHz clock speed
7. Incorporates 3rd party commercial and DoD 3rd party application specific IP
8. Must incorporate full production test capability, including DFT (Design for Test), ATPG (Automatic Test Pattern Generation), designer will provide test vectors, test coverage.

Mixed Signal Chip:

1. > 5M gates (NAND2 equivalent) w/o memory
2. > 10Mb of SRAM
3. At least one controlling processing unit
4. At least 3 high-performance analog elements such as high-performance A/D (Analog/Digital), D/A (Digital/Analog), or SERDES IO
5. Incorporates 3rd party commercial and DoD 3rd party application specific IP
6. Must incorporate full production test capability, including DFT, ATPG, designer will provide test vectors, test coverage.

Digital Design:

1. > 5M gates (NAND2 equivalent) w/o memory
2. At least one controlling processing unit
3. At least 3 high-performance analog elements such as high-performance A/D, D/A, or SERDES IO
4. Incorporates 3rd party commercial and DoD 3rd party application specific IP
5. Must incorporate full production test capability, including DFT, ATPG, designer will provide test vectors, test coverage.

Chiplet:

1. > 5M gates w/o memory
2. Uses AIB (Advanced Interface Bus) and/or AIB-2 interface protocols for IOs
3. Coordinated with the SHIP program for packaging and test
4. Must incorporate full production test capability, including DFT, ATPG, designer will provide test vectors, test coverage.

8. Security Classification, Respondent Restrictions, and other required compliances:

The RFD has been released under Distribution Statement A: Approved for Public Release

The following restrictions apply:

a. Security Classification: Unclassified

b. ITAR Compliance is not required.

c. No additional respondent restrictions are present at this time.

9. Level of Data Rights Requested by the Government

In canvasing the DIB for viable designs and capabilities under this publicized announcement, all submissions received by the Government shall not be disclosed to 3rd parties or non-governmental personnel. Furthermore, no current awardee under RAMP will be granted rights or privileges to a respondents' proprietary information without the express, written approval of the information owner. Respondents may appropriately mark and submit proprietary information (at their sole discretion) to supplement their designs and the RFD Response Worksheet. Respondents shall be entitled to proper protection of their Proprietary Information which includes information and materials designated as proprietary in writing, whether by letter or by use of an appropriate stamp or legend, prior to or at the same time any such information or materials are disclosed to the Government.

For Designs deemed viable and integral to the RAMP Phase 2 Prototype effort, the following rights are anticipated prior to inclusion into any current or future RAMP solutions:

Government Purpose Rights: The right to use, modify, reproduce, release, perform, display, or disclose technical data within the Government without restriction. This also includes the rights to release or disclose technical data outside the Government and authorize persons to whom release or disclosure has been made to use, modify, reproduce, release, perform, display, or disclose technical data for United States government purposes. This level of restriction is set at five-years but may be negotiated & tailored to a specific project.

The five-year period, or such other period that may be negotiated, would commence upon execution of the agreement that required development of the items, components, or processes or creation of the data. The performer will have the exclusive right, including the right to license others, to use technical data in which the Government has obtained government purpose rights under this agreement for any commercial purpose during the five-year period. Upon expiration of the five-year period (or other negotiated length of time), the Government will receive unlimited rights in the technical data and computer software.

Viable designs selected by the Government will be discussed and disclosed with the market respondent prior to any further decision, action or incorporation into any on-going Phase 1 or Phase 2 RAMP efforts. Selection of a viable design does *not* obligate the Government to pay for any information received from the potential sources as a result of this announcement. Furthermore, viable designs may or may not result in a teaming opportunity with a current RAMP awardee, nor should any design selection infer a Government obligation of funds.

10. RFD and Response Process:

Interested parties are encouraged to submit a brief informational statement (no more than 10 pages) on company letterhead, along with responses to the attached RFD Response Worksheet. Please provide any other relevant information that is deemed important to your design(s) and concept(s). The information package shall be sufficiently detailed to assist NSWC Crane in evaluating and determining the viability of the chiplet designs proposed. More than one design may be submitted. Please clearly mark any proprietary information.

The documentation should also provide, at a minimum, the following information:

1. Company Name
2. Address
3. Point of Contact/Title (including telephone number & email address):
4. Design Type: SOC / Mixed Signal / Digital / Chiplet
5. Design Details -

- Program Background
- Technical Description of Design
- Block Diagram(s)
- Commercial IP and DoD IP Descriptions
- Design size
- Memory
- Clocking
- Interfaces
- Input/Output Signal List

Please also include a Rough Order of Magnitude (ROM) cost or price estimate and schedule with your submitted design(s).

11. Response Review:

a. Responses will be reviewed with special attention given to:
   i. Demonstrated expertise and overall technical merit of the response;
   ii. Feasibility of implementation; and
   iii. Design Details and Parameters, cost and schedule

b. The Government will evaluate the degree to which the proposed designs provide a thorough, flexible, and sound approach in response to the subject announcement.

c. The Government reserves the right to reject a submission and deem it ineligible for consideration if the response is incomplete and/or does not clearly provide the requested information. Debriefings will not be provided.

12. Attachments

a. RAMP RFD Response Worksheet

13. Important Dates

a. Questions related to this RFD shall be submitted no later than 12:00 Noon EDT on February 12, 2021.

   To submit any questions, visit the opportunities page at www.nstxl.org/opportunities, select the “Current” tab, locate the respective project, and select “Submit a Question”.

b. Responses submitted in response to this request are due no later than 12:00 noon EDT, Friday, March 5, 2021.

c. To submit your response, visit the opportunities page at www.nstxl.org/opportunities, select the "Current" tab, locate the respective project, and select the "Submit Proposal" link. You must have an active account and be logged-in to submit your response.

d. RFD Respondents are not limited to NSTXL Consortium members; this announcement is open to the public.

14. Additional Project Information

Viable designs may be retained by NSTXL & the Government for possible future informational and market research needs. Non-viable designs shall be discarded and appropriately disposed of to protect any marked intellectual property.