S²MARTS Project 21-07: Rapid Assurance Microelectronics Prototype - Commercial

Request For Solutions (RFS) Questions & Answers | Posted February 15, 2021

Questions related to Fab Companies:

1. Question: You mentioned, its highly encouraged for fabless companies to participate but for commercial viability the needs of DOD programs are very small - comments?

Response: Commercial production volume is required for sustainment of any leading edge foundry as DoD volume is extremely low compared to commercial volumes.

2. Question: What is the role of DoD in ensuring domestic fabs can be competitive and achieve the needed scale?

Response: RAMP-C phase 1 is to assist in the development of IP and PDK as outlined in the RFS. Phase 2 and 3 will require additional government investments as outlined in the 2021 NDAA.

3. Question: While the RFS is not focused on the DIB, can the DIB participate as a sub-contractor to a commercial company?

Response: There are no restrictions on DIB participation; however, the focus is on commercial/dual-use leading-edge solutions.

4. Question: Is it encouraged to have DIB partner on the team?

Response: There are no restrictions on DIB participation; however, the focus is on commercial/dual-use leading-edge solutions.

5. Question: What incentive do fabless companies have to source in the US? How does this program address this?

Response: A few of the benefits could include supply chain security and access, different IP exposure profile and lower susceptibility to geo-political affairs. This program is meant to serve as a pilot to help fabless companies evaluate that possibility through proto-type development.

6. Question: Does a Fabless company need to team with a fab to make a response? Will you be providing fab teaming introductions?

Response: Either team or be able to demonstrate a business relationship showing collaboration across all the tasks. The Government will not be making introductions and would request that those companies work together for a complete solution.

7. Question: For fabless companies willing to participate - is the expectation to use the SHIP approved packaging and test center?

Response: The use of the SHIP approved packaging and test center is not required.

8. Question: For fabless companies that are not on US Fab nodes (but have their products on much advanced nodes) what are your comments?

Response: Per the RFS we are seeking on-shore nodes ≤ 7nm.

9. Question: Are fabless company design team(s) able to lead a RFS response?

Response: Yes, as long as the full team is able to meet the full RFS requirements and all sub-phases.

Questions related to Technology Node and SOTA

10. Question: What is the definition of leading edge CMOS? What node is required?

Response: Per the RFS < 7nm, and that is what is required.

11. Question: How is ITAR and government flow related to commercial access? Do we already have commercial access to SOTA?

Response: The majority of chips used in DoD systems are not ITAR, they are dual-use COTS. This effort is to enable access to an on-shore leading foundry (≤ 7nm) for supply chain risk reduction.

12. Question: When does this SOTA capability have to be available for production?

Response: The production is outside of the scope of this OTA effort. Phase 2 and Phase 3 are briefly mentioned and will be dependent on additional funding as described in the FY2021 NDAA.

13. Question: Please define OSD view of US SOTA, based on current us landscape

Response: Definition of SOTA as was used in the RAMP RFS is ≤22nm, definition of leading edge per the RAMP-C RFS is ≤7nm.

14. Question: What level of maturity must the US based foundry have for 7 nm and below? Must it already have a commercially release process?

Response: For phase 1, the maturity would be that of a foundry bring-up for initial test chip for evaluation. This would transition to a maturity level supporting high commercial volume production by the end of phase 3.

15. Question: Is the expectation that the model developed for digital CMOS would then also be applied to other technologies of domestic interest?

Response: That is possible if a successful public-private partnership can be demonstrated as a viable model for other critical areas of interest.

16. Question: What is a commercial foundry? What ECCNs need to be supported?

Response: The foundry model would be that of a pure play or merchant foundry available to produce product for multiple fabless design companies. As commercially operated foundry focused on COTS and dual-use parts, EAR99 would apply, however specific designs being produced might have to be evaluated for any restrictions.

17. Question: what node is considered SOTA?

Response: Definition of SOTA as was used in the RAMP RFS is ≤22nm, definition of leading edge per the RAMP-C RFS is ≤7nm.

18. Question: Please define SOTA relative to us landscape

Response: Definition of SOTA as was used in the RAMP RFS is ≤22nm, definition of leading edge per the RAMP-C RFS is ≤7nm.

Questions related to Quantifiable Assurance:

19. Question: Describe your view of integration with RAMP, from design to QA.

Response: While RAMP is focused on Government purpose use chips, QA methods and processes developed under RAMP could be applicable to RAMP-C. However, these is no direct requirement in the RAMP-C RFS to implement specific QA methods and processes.

20. Question: The RFS mentions quantifiable assurance. Will the gov't provide the QA framework, or is the RFS seeking innovative QA solutions as a component of our response?

Response: The Government is developing standards and supporting information that will be made available to the RAMP-C performers. A primary objective of RAMP-C in this area will be to understand and leverage commercial best practices used to optimize yield and reliability and apply for ensuring integrity and confidentiality.

21. Question: Should we assume QA is defined by RAMP?

Response: No, RAMP is addressing Government specific designs while RAMP-C is addressing commercial dual-use chips. These are different operational risk models and design/production flows.

22. Question: The RFS mentions quantifiable assurance. Will the gov't provide the QA framework, or is the RFS seeking innovative QA solutions as a component of our response?

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23. Question: Does the incorporation of Quantifiable Assurance imply OSD's desire to use QA processes and technologies already developed by the government? Thank you.

Response: see question 19, 20, 21 and 22.

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Questions related to RAMP and/or SHIP:

25. Question: If you are a newcomer to RAMP/RAMP-C, must formal relationships be established prior to proposal submission?

Response: Formal relationships would not be required but the Government would encourage some type of business arrangements be made in order for these two programs to better align to objectives such as discussed in the area of QA .

26. Question: How does the political situation (new govt) affect this RAMPC initiative?

Response: There has been no impact on the RAMP-C RFS or objectives.

27. Question: With RAMP RFD , is there synergy with RAM C plan

Response: There could be depending on purposed teaming and selected performers, but that is not a requirement from the RFS.

Questions related to Schedule/Award:

28. Question: WHAT Is the SCHEDULE for submission?

Response: Proposals are Due 17-March.

29. Question: I have heard that the schedule has been extended beyond mid feb

Response: Yes, extended to 17-March.

30. Question: Will there be multiple awards?

Response: Currently not planned but the Government has the option to fund multiple awards based on funding and responses.

31. Question: What is the schedule for answers to other submitted questions?

Response: Answers will be provided on the website as soon as possible. Planned date is 8-February.

Other Questions:

32. Question: Will DoD be able to sustain this long-term?

Response: The reason to team with fabless design companies is to enable sufficient commercial volume for sustainability and to give them an on-shore option.

33. Question: What state of maturing must the PDK be for using in the design? Must the PDK already be released commercially?

Response: A PDK matured for commercial use would be ideal for lowing risk and shortening development time.

34. Question: We have heard that ITAR/ classified info capabilities aren't required. The DD 254 includes language contradicting that assertion. Will an update be put out?

Response: The DD254 and ITAR/Classified capability is not required at award. This DD254 was put in place as an option for sponsoring security clearances for counterintelligence and supply chain threat focused discussions if necessary. Proposers do not need to demonstrate the ability to receive or generate ITAR or classified information to be considered for an award.

35. Question: Should custom IC design teams/groups from defense Primes submit, if so in what role?

Response: They would have to team with a commercial fabless design company or otherwise provide sufficient expertise and experience to address a given task.

36. Question: What standards and market incentives are tied to this project? What is the status of Sec. 224

Response: The Sec 224 standards are in development and a draft version will be shared with the performer once under Gov contract. The standards will be made widely available once they gave gone through the formal Gov issuance process.

37. Question: Is the intent to reshore existing design to a US foundry, or new designs/next generation designs not yet approaching production?

Response: It could be either as long as it targets a $\leq$7nm node with the potential for high commercial production volume.

38. Question: Are there military reliability or environmental requirements that need to be addressed?

Response: The proto-types developed would have to meet commercial requirements for that particular product. Depending on application, it could have more demanding requirements such as automotive.

39. Question: Is there any role for the DIB for RAMP-C?

Response: There are no restrictions on DIB participation; however, the focus is on commercial/dual-use leading-edge solutions.

40. Question: Are foreign nationals (including Chinese nationals) allowed to participate on these design teams?

Response: There are no restrictions on foreign nationals.

41. Question: Does the requirements for a US based foundry include having the IC masks made in the US?

Response: Yes.

42. Question: RFS page 11 mentions Task 4 sub-phase 1a-1d as $20M per design (3 designs). Is this 3 testchip designs?

Response: The requirement is 1 test chip design per design team.

Supplemental Question & Answer Responses (2/15/2021):

Note: These responses are for residual questions that weren't originally answered during the 2/8/21 release.

A. Question: Can proposers respond to less than all tasks?

Response: Proposing teams may propose to one or more tasks and be considered for selection and funding. However, proposals addressing all tasks collectively are preferred. All proposals will be evaluated according to the metrics for each task listed in the RFS. Proposals for individual tasks must demonstrate business relationships with all the other task performers to ensure a comprehensive solution.

B. Question: Can proposers respond to Quantifiable Assurance as its own task?

Response: Proposals must satisfy the requirements for one or more of the tasks listed in section 5 of the RFS. Quantifiable Assurance is part of each task and cannot be considered as a separate, independent task.

C. Question: Can proposers propose additional test chips beyond the one test chip mentioned in the RFS?

Response: The intent of the test chip mentioned in the RFS to: 1) permit hardware verification of foundation, 3rd party, and design-specific digital and mixed-signal design modules (IP) and 2) exercise the full enablement infrastructure in preparation for full product design and fabrication in Phases 2 and 3. The test chip number and schedule should be considered informational to proposers and not proscriptive.

D. Question: Will Performers be required to verify foundation IP and 3rd party IP through test chips?

Response: Yes, this is standard industry practice.

E. Question: For many different types of IP (especially memories and analog/mixed signal ones) the norm is to have multiple test chips and tapeouts to qualify/validate the IP before integration into a system. Upon reading the call it appears that one tapeout is planned at the end of the Phase I directly into

partners' systems. Are there any provisions for earlier MPW shuttles for isolated IP testing/qualification?

Response: Test chip is not intended to go into partner systems. It is a test chip to evaluate IP modules as well as the efficiency of the enablement ecosystems.

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G. Question: The description that is provided for the 3rd party IP track suggests targeting analog/mixed-signal IP (possibly PHYs). Are hardened digital IP macros of interest if they present some unique capability? Is soft IP (in RTL form) of any interest (for example due to assurance criteria) or is the expectation that all soft IP will be licensed from existing IP vendors (since it is presumably process agnostic)?

Response: Normal commercial practices should be followed fo creating IP for a new foundry node.

H. Question: Could multiple testchips be awarded to a single fabless company?

Response: We only expect to award one test chip design per fabless company.

I. Question: Are companies required to provide all IP developed in RAMP-C with Government Purpose Rights?

Response: Government rights to IP (design modules, technology, etc.) developed as part of RAMP-C will be defined as part of contract negotiations after proposal selection and is dependent on the origin and role of each piece of IP. The government understands that it may not be appropriate for the government to assert Government Purpose Rights for some IP.

J. Question: Do all fabless design company and 3rd party IP provider work need to be aligned to a specific wafer foundry?

Reason: The intent of the RAMP-C is to develop the complete design and fabrication ecosystem to support a U.S. located wafer fabrication facility for use by commercial and DoD entities. As a result, any design activities (product design, 3rd-party design, or Foundation IP design) need to be strongly connected with and support a given U.S. located foundry capable of providing leading-edge CMOS fabrication.

K. Question: What assumption should a fabless company use as to which foundry company will create the technology?

Response: A fabless company will need to have a design plan that is supported by a particular foundry.

L. Question: Will pairing be facilitated between fabless companies and foundry companies for a joint bid?

Response: The preference is for teaming to be done prior to award and the Government will not be facilitating the arrangement.

M. Question: Is the expectation that multiple foundry ecosystems will result from this program?

Response: RAMP-C is expecting to develop a single U.S. located foundry ecosystem.

N. Question: Does the Government expect to provide additional information and requirements regarding Quantifiable Assurance in time for Performers to consider scope, schedule, and price impacts in their proposals?

Response: This is possible because a QA primer has already been developed. However, it is probably not advisable due to the short response time.

O. Question: What is meant by Initial Operating Capability (IOC) & Full Operating Capability (FOC)?

Response: Initial operating capability is the state achieved when a capability is available in its minimum production capability. Full Operating Capability is full production capability equivalent to at volume commercial level production.

P. Question: Is the Quantifiable Assurance method defined in RAMP-C expected to be based on RAMP or is any QA proposal allowed?

Response: The Quantifiable Assurance method implemented for RAMP-C will be based on DoD policy/standards as well as advances developed in RAMP.

Q. Question: We will package LV MOSFETs as a chiplet module using existing dies. In this package will also be: HV CMOS logic, drivers and mixed signal features using a mixture of 1u, 0.8u and 0.35u. These nodes or gate lengths are ripe for immediate SoC integration as they are numerous in the discrete design which can be further optimization, demand high production volumes and there are both IPR and fabs available in USA. Will this chipset development and prototyping fit for your program combined with AFWERX Microeconomics Prime?

Response: The RFS states develop capability to design and manufacture into a <7nm process

R. Question: Is the $310M budget only for Phase 1?

Response: Yes

S. Question: Section 9, "All of these requests should be incorporated in the easy-to-use, data-driven database for use by a novice circuit designer." Is this database a deliverable of the program or does it refer to something else?

Response: This could take the form of a cloud-based repository with access restricted to those with use agreements in place. Existing cloud-based solutions should be leveraged as it not the intent of this RFS to create a new database repository from scratch.

T. Question: Certain quantifiable assurance methods come from the DIB, are those in scope for RAMP-C?

Response: Quantifiable Assurance efforts are included in each individual task and is not a separate task.

U. Question: A goal is for the DIB to have access to domestic leading edge technology, when/how will that introduction occur?

Response: RAMP-C focuses enabling on-shore leading edge foundry capability. Once this is operational, the DIB would have access via shuttle runs.

V. Question: Paragraph 2: The second paragraph does not appear to be a standard provision. Can you confirm that it has been intentionally included, if it can be removed, or otherwise excepted?

Response: Those details would be refined during the post-selection negotiation talks

W. Question: Delivery vs. Licensing: Section 9, Paragraph 2 lists data and other IP that the Government wants delivered. Does the Government intend to enumerate those items as deliverables in the contract (e.g., in a CDRL)?

Response: Those details would be refined during the post-selection negotiation talks