S²MARTS Project 20-06: Rapid Assured Microelectronics (RAMP)

Request for Solutions (RFS) Questions & Answers | Posted April 27, 2020

78. Question: Has the physical design requirements aimed at advanced node been already implemented in older nodes Like 65nm or 45nm for DOD needs?

Response: RAMP is focused on SOTA (< 22nm), and while the intent of RAMP is not to specifically port previous designs, if IP from those designs is needed for demonstrating the RAMP design flow and target application, then partial IP reuse is acceptable.

79. Question: Do you anticipate a new device fabrication or implementing a new flow on already existing Silicon platforms like advanced node FPGAs?

Response: A new device fabrication is expected using a SOTA (<22nm) foundry.

80. Question: Are the performers to propose designs or will the government provide the chip designs?

Response: The performer should propose designs in collaboration with the DIB or DoD Program offices. The DoD evaluation team will participate in the selection process, and reserve the right to provide designs if needed.

81. Question: How will the implementation of 5G affect RAMP development?

Response: RAMP is looking to develop the back-end design methodology to enable assurance for access to SOTA ICs manufacturing, which can be applied to multiple applications and implementations.

82. Question: How will RAMP affect legacy systems?

Response: RAMP is not meant to be a legacy replacement. If a design does not need SOTA they should not use RAMP, since it would be more expensive.

83. Question: In one of your chart, it seems to indicate confidentiality is applicable only on design phase and integrity only on fabrication phase. Is this correct?

Response: That was not the intention. Both Confidentiality and Integrity applies to the entire manufacturing/fabrication process, which includes the capability that RAMP is addressing.

84. Question: Is RAMP looking for novel methodology or secure SOTA ICs?

Response: RAMP is looking to develop the back-end design methodology to enable assurance for access to SOTA ICs manufacturing.

85. Question: Can you clarify the classification of Phase 1 & 2?

Response: The Security classification for this program is Unclassified. Controlled Unclassified Information (CUI) is an umbrella term that encompasses all Covered Defense Information (CDI) and Controlled Technical Information (CTI). As stated in Section 8.a.:

- Respondents must be compliant with DoDI 8582.01, "Security of Unclassified DoD Information on Non-DoD Information Systems" and DoDM 5200.01 Volume 4, "DoD Information Security Program: Controlled Unclassified Information."

- Respondents must implement the security requirements in NIST SP 800-171, "Protecting Controlled Unclassified Information in Non-Federal Information Systems and Organizations."

Respondents are expected to receive, generate, and handle CUI in accordance with DoDI 8582.01, DoDM 5200.01, and NIST SP 800-171. CDI includes:

(1) Marked or otherwise identified in the contract, task order, or delivery order and provided to the contractor by or on behalf of DoD in support of the performance of the contract
(2) Collected, developed, received, transmitted, used, or stored by or on behalf of the contractor in support of the performance of the contract.

86. Question: Is the expectation to deliver a cloud-based design platform that allows effective collaboration among DIB, Foundries, EDA and commercial partners?

Response: A cloud based platform is not required, but it would be a desirable option.

87. Question: When will more detail related to (referenced in the RFS on page 2 #5) be provided?

Response: There will be no Phase III and it will be removed from the RFS.

88. Question: Does the RAMP ecosystem should produce IC designs that are resilient to post fabrication attempts to cypher sensitive information

Response: Confidentiality is important and this would be a desired feature.

89. Question: Is the proposer required to propose both Phase 1 & 2 at this time? or only Phase 1 should be proposed?

Response: Respondents should provide their Statement of Work (SOW) for this effort and a cost proposal for Phase I with ROM estimates for following phase.

90. Question: Is a program of record "Sponsor" required for the proposed designs?

Response: A program of record "Sponsor" is not required for proposed designs, but all three designs must be DoD relevant.

91. Question: Can you go into more detail about how RAMP and SHIP will interact and the role of non-trusted foundries in this process?

Response: RAMP and SHIP are independent programs. If the RAMP designs are chiplets for multi-die packages, there could be interaction related to testing and quantitative assurance, otherwise no direct interaction.

92. Question: Do you have further definition of "a secured design" means?

Response: A secure design is safe and protected, such that the design cannot be compromised during any step in the design process.

93. Question: RFS Section 5 (Desired End-State Objective(s) & Success Criteria) makes reference to a "Phase 3 ". Is that art of the current or future program?

Response: There will be no Phase III and it will be removed from the RFS.

94. Question: Do you anticipate additional funding to be provided in phase 2 to enable multiple chip designs?

Response: The $50M is anticipated for multiple phase I awards. Additional funding will be available for Phase II.

95. Question: Section 9 talks about delivery of all IP. What is the position on delivery of IP from foundries and EDA vendors that was created outside of this program?

Response: The government is requesting a complete data package that will enable any form of independent analysis including failure analysis of parts as well as long-term obsolescence management. Generally speaking, our requested data rights are flexible, and any offeror can suggest rights that they think are appropriate. While a minimum set of IP rights to info that we feel is critical, we will leave open the possibility of negotiating changes before phase 2.

96. Question: SotA foundries / foreign governments often want assurance chips will not be used in WMD etc. Will this be a separate area of effort for DoD to resolve?

Response: There should be no restrictions on use in DoD weapon systems, including potential use in nuclear weapon systems.

97. Question: This program is listed for $50M but the requested scope exceeds this cost model, will there be a means to reconcile post award?

Response: The $50M is anticipated for multiple phase I awards. Proposals should be scoped appropriately leveraging existing commercial capabilities to the greatest extent possible. Additional funding is available for Phase II.

98. Question: What will be the role of TAPO that will play in the future or will completely phase out?

Response: Any existing TAPO capabilities that could support the RAMP objectives can be considered. The future of TAPO is outside the scope of RAMP.

99. Question: In phase 2 fabrication will be provided by the government or need to be costed?

Response: Fabrication costs are not guaranteed by the government, however there may be opportunities to participate in MPW runs, depending on the target foundry and process. Initially it should be included in the Phase 2 ROM and will be further refined during the Phase 2 contract SOW and metrics negotiations.

100. Question: What is the government's position on prior background IP for demonstration SoC designs for prototyping, relative to program Data Rights Requested (Section 9)?

Response: The government is requesting a complete data package that will enable any form of independent analysis including failure analysis of parts as well as long-term obsolescence management. Generally speaking, our requested data rights are flexible, and any offeror can suggest rights that they think are appropriate. While a minimum set of IP rights to info that we feel is critical, we will leave open the possibility of negotiating changes before phase 2.

101. Question: RAMP will use commercial design IP libraries compatible with TSMC?

Response: RAMP will use commercial design IP, including PDK's, for the target foundry and process. (See question 7)

102. Question: Are designs expected to be fabricated and tested during Phase 2 and if so will MPWs be provided by the government?

Response: Fabrication costs are not guaranteed by the government, however there may be opportunities to participate in MPW runs, depending on the target foundry and process. Initially it should be included in the Phase 2 ROM and will be further refined during the Phase 2 contract SOW and metrics negotiations.

103. Question: There are companies that provide some of RAMP capability. The 6mo period of phase 1 implies advantage to those companies. Are you open for newcomers?

Response: RAMP is open to all whom can meet the objectives.

104. Question: Does RAMP prototype performance capability mentioned augment the solicitation requirement that the prototype demonstrate Phase 1?

Response: Per the RFS, "The primary objective of the project is to leverage the expertise of commercial industry to develop and demonstrate a novel capability for design of State-of-the Art (SOTA) (defined as ≤ 22nm node Si CMOS) ICs and System On a Chip (SoCs) microcircuits that can be designed and verified in the most advanced semiconductor processes. In addition, a RAMP prototype will achieve lower power consumption, improved performance, reduced physical size, and improved reliability for application in DoD systems."
Access to SOTA processes is a primary driver to enable greater performance, size, and power.

105. **Question**: The focus was stated to be physical design (place & route). Does this exclude front-end design in the environment for confidentiality/integrity techniques?

Response: This does not exclude any recommendations for confidentiality/integrity recommendations for front end design.

106. **Question**: Can you provide industry with visibility to the threat model to build a broader class of solutions or will this only be shared with contractors?

Response: There is currently no plan to provide industry with the threat model until Phase 1 performers are selected and contract awarded.

107. **Question**: How to provide DoD performance differentiation over adversaries, if everyone access to the same foundry technologies and commercial design IPs?

Response: The DoD can still develop their own IP for designs.

108. **Question**: Do you envision a "Design Center" to be created that is the focal point for the DIB to go to for SOTA design assistance and fab enablement?

Response: That would be the desired outcome for the DIB to use RAMP for future SOTA (<22nm) designs.

109. **Question**: If there is no implementation required in phase 1, what is expected in the proposal on 5/29? pls confirm that phase 1 deliverable is a report not a platform?

Response: Establishment of Secure Design Capability that supports an enhanced physical design by the DIB in SOTA (defined as ≤ 22nm node Si CMOS) technology nodes.

110. **Question**: How many award are anticipated for Phase 1 and Phase 2?

Response: No decision on how many awards will be made until the proposals are reviewed by Government evaluation team.

111. **Question**: Does Mr. Hamilton's comment regarding the RAMP prototype performance capability augment the solicitation requirement that the prototype demonstrate Phase 1?

Response: Per the RFS, "The primary objective of the project is to leverage the expertise of commercial industry to develop and demonstrate a novel capability for design of State-of-the Art (SOTA) (defined as ≤ 22nm node Si CMOS) ICs and System On a Chip (SoCs) microcircuits that can be designed and verified in the most advanced semiconductor processes. In addition, a RAMP prototype will achieve lower power consumption, improved performance, reduced physical size, and improved reliability for application in DoD systems."
Access to SOTA processes is a primary driver to enable greater performance, size, and power.

112. **Question**: Will the rest of the questions submitted by the 27 April noon deadline be answered?

Response: Yes, the questions and answers will be posted.