The intent of the Microelectronics Commons is to establish a network of regional hubs to evolve laboratory prototypes to fabrication prototypes (lab-to-fab). In particular, innovative prototype demonstrations in microelectronics materials, processes, devices, and architectural designs will be supported. Peripheral activities pursued as stand-alone topics are not within scope of the Commons hubs unless they are essential for lab-to-fab demonstration of the prototype.

Activities executed within Microelectronics Commons shall primarily fall under Budget Activity 3. Although activities that fall under Budget Activities 2 and 4 will also be supported if they are in support of the lab-to-fab prototype. For further discussion on research, development, testing and evaluation (RDT&E) budget activities, see https://comptroller.defense.gov/Portals/45/documents/fmr/archive/02barch/02b_05old.pdf. For further discussion on Technology Readiness Levels (TRLs) referenced in the Budget Activities document, see https://apps.dtic.mil/sti/pdfs/ADA418881.pdf. For further discussion on Manufacturing Readiness Levels (MRLs), see https://www.dodmrl.com/MRL_Deskbook_V2.pdf.

The Commons will support prototyping capabilities for six technical areas that are critical to the DoD. Those areas are: Secure Edge/Internet of Things (IoT) Computing, 5G/6G Technology, Artificial Intelligence Hardware, Quantum Technology, Electronic Warfare, and Commercial Leap Ahead Technologies. The below desired end-state prototype descriptions are provided as technical guidance for the advancements needed in each technical area.

A. Secure Edge/IoT Computing Hubs Desired End State

The desired end-state of secure edge computing is the prototyping of microelectronics technologies based on lab-to fab transition of novel materials, devices and architectures that enable future mission security and assurance. The rapid proliferation of autonomous systems requires more capable computing technologies to drive the performance, assurance, and resilience needed for the contested threat environments of the future. The integration of these elements into national information systems for edge computing will protect the integrity, confidentiality, and availability of our information systems by preventing the loss of control, exfiltration, or manipulation of our Critical Program Information (CPI), deterring adversaries, and providing a means to react in all circumstances.

Secure processing architectures with varying input/output (I/O), processing capabilities, and size, weight, and power (SWaP) plus security (SWaP+S) constraints are required to meet multiple needs of DoD Industrial Base. The development of a general-purpose secure processing architecture that meets the requirements of many mission threads is a priority with additional architectures developed for more stringent/lenient SWaP+S constraints. Secure edge computing also requires the development of space-targeted secure processors. Secure processing architectures will be designed to utilize state-of-the-art technology that can advance and demonstrate lab-to-fab prototyping, and other fabrication facilities as applicable to air, space, and terrestrial domains. New approaches to edge computing must holistically consider the functionality of the platform.

Properties desirable for secure edge computing include, but are not limited to, 1) advancements in SWaP+S metrics required for future edge computing assets; 2) physical and cyber protection capabilities to provide a holistic security posture to protect the control flow of the processor from external influence, ensure the integrity of the system during execution, prevent exfiltration of information and CPI, and

provide a means to recover from threat events; and 3) capabilities to pair secure processors with untrusted high performance computing elements.

It is re-highlighted that peripheral activities pursued as stand-alone topics are not within scope of hubs unless they are essential for lab-to-fab demonstration of the prototype. Some of these activities may include 1) design for testability and verification, 2) innovations and enhancements in cyber and physical defenses, 3) unique modifications to software and algorithms to take advantage of performance and the security features of the hardware components, and 4) new technologies enabling resiliency in operational environments. Advances being sought include but are not limited to the following:

Advances in SWaP Computing Approaches
Edge computing requires new approaches to reducing SWaP on battlefield platforms for fast decision-making. Solutions may include 1) computation before the sensor to reduce processing power and time, 2) on sensor computation, and 3) novel approaches to high-density storage, algorithms to better identify relevant data, and more efficient methods for communication among sensors. Example lab-to-fab microelectronics solutions for this hub include, but are not limited to, disruptive advances in SoTP/ SoTA digital fabrication processes for secure ADC/DAC and memory applications. These advances are necessary as the DoD shifts toward digitizing sensor data with increased processing power. Innovations in new materials, devices and architectures are also sought for disruptive energy and performance efficiencies. These include but are not limited to non-silicon based processing as well as novel memory, processing or Tensor architectures.

Advances in Hardware/Software Co-design and Integration
Secure edge computing platforms generally share a set of desirable characteristics that include hardware assurance. Low SWaP and cost (SWaP+C) devices and certain operating conditions may impose constraints; therefore necessitating solutions that scale to the resources available, as well as a distributed trust model to generate and share trustworthy data. Proposed architectures for fault tolerance, redundancy, diversity, recovery, monitoring, and remote attestation must be validated. Further, new processes must incentivize a "multi-acquisition-program" view of custom system-on-chip (SoC) advantages and distinguish between IP core access and ownership, thereby paving the way for hybrid designs, IP core reusability, and shared repositories that protect critical design information and industrial IP.

B. 5G/6G Technology Hubs Desired End-State

The desired end state of Microelectronics Commons 5G/6G hubs is integrated, resilient, low-latency Command and Control (C2) and communication infrastructure and protocols. Future Generation (5G/6G) radio frequency (RF) technology advancements are critical for the DoD to transition to decentralized, point-of-use, anytime-anywhere RF networks that yield asymmetric DoD warfighting results. The implications of 5G/6G are potentially revolutionary by connecting a wide variety of DoD platforms into a secure network that must remain protected from our adversaries. Future Generation RF connectivity is predicated on secure, efficient and broadband RF microelectronics technology in the RF, microwave, and millimeter-wave (mmW) bands from 0.3-300 GHz. As the complexity and capability of modern warfare grows, facilitated by enablers such as Artificial Intelligence (AI), the amount of data and processing speeds required to support future missions must be bolstered by high bandwidth real-time architecture, highlighted by Joint All Domain Command and Control (JADC2) initiatives.

The desired end-state for 5G/6G technology hubs consists of microelectronics solutions addressing 1) disruptive advances in RF power microelectronics for transmit and receive functions in narrow-band, broad-band and high-linearity communications in the RF, microwave, and mmW bands; 2) ultra-efficient RF integrated circuit design topologies delivering communications solutions for power dense systems; 3) software defined networks unconstrained by commercially driven protocols and parameters, resulting in 4) secure, point-of-use, low-latency, and high-speed data rate communications chip-sets capable of integrating terrestrial and non-terrestrial DoD platforms. Future 5G/6G hubs should support agile

waveforms and dense, cost-effective scalable networks with ultra-high speed links to the tactical edge for future autonomous battlespace needs. In addition, solutions are sought to achieve:

Advances in RF power microelectronics component technology
A core capability of 5G/6G networks is the ability to achieve RF transistor gain over a broad frequency range from 0.3-300 GHz to support current and future generation networks. For military applications, communicating between ground, air and space-based assets requires high RF power and high-linearity over broadband. At mmW frequencies, unique challenges such as increased power density and reduced gain lead to inefficient operation. Prototype demonstrations of RF microelectronics should focus on achieving high gain solutions and survivability in extreme conditions such as high-temperature and radiation environments. Compound semiconductors, ranging from narrow to ultra-wide bandgap, offer electrical properties possessing many of these niche DoD requirements.

Advances in efficient RF integrated circuits
Demonstrated lab-to-fab RF microelectronics solutions at the circuit level can be implemented to overcome lower power transistor efficiency at mmW frequencies. For example, integrated RF microelectronic circuits utilizing harmonic tuning, load modulated balance, envelope tracking, and other waveform engineering solutions are of interest to increase chip-level efficiency for DoD platforms as is autonomous frequency agility/tunability for operation in spectrally challenged environments.

Advances in Hybrid Microelectronic and Photonic Integrated Circuits
To meet the demands of future 5G/6G applications, enhancements in hybrid microelectronic and Photonic Integrated Circuits (PICs) are required. Innovations in interconnect technology between chiplets, FPA/ROIC bonding, optical components, and monolithic microwave integrated circuits enables integration of ME within system SWaP constraints, as well as facilitates agility to meet mission requirements. Novel advances will also ensure hybrid circuits will be able to survive harsh environments typical of DoD platforms.

Advances in emerging platforms for secure point-of-use DoD data networks
In order to meet future 5G/6G demands, chip I/O bandwidth must be enhanced, specifically in two areas: (1) internal computational efficiency, and (2) external data transfer from one site, or High-Power Computing (HPC) unit, to another.

Specifically, node-to-node bandwidth is a major driver in recovering computational efficiency. Novel chip development and system integration of co-packaged optical I/O is required to realize this bandwidth. Some examples include, but are not limited to, mmW direct conversion RF front ends, as well as technologies for accessing alternate spectrum and providing anti-tamper mechanisms including RF-photonic circuits, photonics components as well as devices that can leverage optical polarization. Similarly, high-speed networking capability will result in additional technical challenges to bring 5G/6G system level performance down to package scale, affordable at DoD levels.

C. Artificial Intelligence (AI) Hardware (HW) Hubs Desired End-State

The desired end-state is a fab prototype for eventual deployment in AI-enabled systems for edge applications to enable overmatch performance in operational situation awareness and decision-making in a wide variety of missions. Microelectronics Commons hubs will need to facilitate the lab-to-fab prototyping and testing of these AI hardware platforms.

The exponential growth of data demands advanced data analysis capabilities with higher processing performance, lower energy dissipation, and better system scalability. There is a significant gap between current AI computing capabilities and the vast amount of multi-domain sensor and operational data for high-throughput, low-latency and energy-efficient training and executing (inference) of AI models for data analytics, sensor exploitation and fusion, decision support, autonomy, etc., particularly for systems at

the tactical edge where there are strict SWaP constraints. Furthermore, the current state of main-stream AI models and their underlying computing architectures do not enable rapid adaptation to changes in the actual sensor/operational data and environments, leading to degraded real-world performance such as intolerance to subtle changes in inputs (i.e., brittle) and difficulties in transitioning to a new task or environment (i.e., inflexible). Existing AI solutions also lack the appropriate computing architecture/hardware, and subsequently, algorithmic innovations to timely search decision space under complex situations and constraints, generate optimized course-of-action recommendations, and interact-learn-assist the human in decision-making.

Few commercial off-the-shelf hardware options exist today for AI edge applications. Most reduce the time required to train large deep neural networks. These current hardware options fall into two categories. The first involves specialized hardware designs (e.g., Google TPU, Qualcomm NPU) that implement optimized operations for training. The second use neuroscience-inspired designs. For example, neuromorphic chips (e.g., IBM TrueNorth, Intel's Loihi series) have performed effectively for applications involving mobile robotics, small maritime platforms, and space systems. However, they are not widely available because (1) a strong motivating (commercial) application need has not yet arisen, and (2) further study is needed to increase their performance.

Current industry advances were designed to capture a large consumer base. While they offer flexibility, it often results in lower efficiency and limited ability to tailor the processors to specific applications, architectures, and interfaces. Hubs should facilitate the lab-to-fab prototyping of multiple emerging AI accelerators. The following advances are needed:

Advances in High Performance, Energy Efficient, Reconfigurable, and Scalable Hardware
Innovative prototype demonstrations of novel computing architectures with hardware instantiations that achieve unprecedented computational performance and energy efficiency are needed. Reconfigurable hardware to address emerging requirements and simple integration with existing platforms for a wide array of operational environments are also needed. Finally, new AI-optimized hardware to address low-power Systems-on-Chip (SoC) to high-performance server implementations is also needed.

Advances in Emerging AI Processing Hardware
Innovative prototype demonstrations of hardware for AI inference, adaptive AI learning, and AI optimization are needed. In addition to achieving high computational performance and energy efficiency and allowing simple integration into existing platforms, AI inference hardware that allows implementation of a broad variety of AI applications is needed. The capability to enable rapid and adaptive AI learning from new, unstructured stimuli is also needed. Finally, AI optimization hardware should timely solve some of the most challenging problems for traditional processors (CPUs/GPUs) to support an array of course-of-action applications.

Advances in Test and Measurement Capability
Test capabilities must be available to evaluate AI hardware performance, efficiency, throughput, affordability, and SWaP under real load conditions. To the extent possible, existing test and measurement capabilities should be leveraged. Development of new test and measurement capabilities should not be the focus of AI Hardware hubs.

Advances in Software Stack for AI Chips
A full end-to-end, *co-designed*, high-productivity software ecosystem is required for maximizing hardware system performance and efficiency. Energy-efficient AI domain-specific processors cannot operate without the support of full toolchains. Software development is supported by commercial industry. Therefore, at this time, AI Hardware hubs should focus on developing hardware prototypes.

Neuroscience-Inspired Designs

Computing performance advances from future complementary metal-oxide-semiconductor (CMOS) technologies will likely be limited due to the end of Moore's Law. In addition, intrinsic limitations of the Von Neumann computing architecture, a.k.a. the "memory wall", are prohibiting AI computing platforms from meeting future data-to-decision and autonomy requirements. These limitations have motivated emerging research areas in neuromorphic computing that is inspired by the architecture and working mechanism of the human brain. At least four capability gaps must be closed before neuromorphic chips can be deployed widely in DoD applications. First, current architectures include only a small number of "neurons," preventing them from satisfying the needs of computationally intensive AI edge applications. Second, these chips must operate in real-time, much like cell phones and autonomous vehicles. Third, neuromorphic chips have a SWaP advantage versus those based on the von Neumann architecture but must be scaled in complexity while satisfying size, weight, and power constraints. Finally, novel, in-situ characterization methods will be required. The ability to deliver prototypes of novel chip designs for supporting AI-enabled edge applications will require the following advances:

Advances in Materials and Fabrication Processes
To date, neuromorphic hardware has been implemented primarily on silicon chips. To unleash the true potential of this hardware, advances in novel nanoelectronics, nanophotonic materials, memristor architectures, and fabrication processes are required to allow the development of platforms that realize the full potential of brain-inspired neuromorphic computing. These advances have the potential to satisfy many of the limitations that prevent the current use of neuromorphic chips for AI edge applications.

Advances in Neural Network Architectures
Neural network computing schemes utilize many-to-many connectivity to achieve computational tasks that evade conventional digital computing. However, a physical interconnection architecture to match that of biological neural networks has not been devised for novel nanoelectronics-based neuromorphic devices. The conventional interconnect method of defining lithographically patterned metallic lines in two-dimensional planes is unable to generate a large number of connections beyond a few nearest and next-nearest neighbors. Additional connections require additional lithography steps, at linearly increasing fabrication cost and with diminishing returns in terms of actual connectivity increase. Crossbar structures, while enabling many-to-many connections, suffer from crosstalk between adjacent lines. The address-event representation (AER) protocol used in silicon-based neuromorphic chips, a time-multiplexing scheme, is capable of flexibly enabling massive neuro-synaptic interconnections but requires a digital interface and data exchange with remote memory, retaining the inefficiencies of the von Neumann computing paradigm. Both crossbar and AER architectures fail to replicate the variety of spike arrival timing information that arises from the length and impedance differentials of biological dendrites. The lack of an architecture to achieve a large number of diverse and unique physical interconnections is a critical factor preventing novel beyond-CMOS neuromorphic computing devices from reaching their full potential as enablers for complex cognitive systems. The development and fab prototyping of such an architecture is imperative to fully realizing the advantages to be gained from nanoelectronics-based neuromorphic hardware.

Advances in CMOS Integration of Novel Neuromorphic Materials
For a neuromorphic chip to interact with its edge platform, it must be integrated with sensors, actuators and control modules via silicon-based CMOS circuitry. This integration is complex, requiring context dependent customization and adaptation that the industry's semiconductor pipeline does not provide. AI Hardware hubs will need to accommodate a flexible, streamlined lab-to-fab development pipeline to facilitate the production of novel ready-to-use neuromorphic chips.

Advances in Co-Design

Hardware designs constrain the capabilities of software they execute, while software places requirements on the supporting hardware. Given this, hardware/software chip *co-design* methods are encouraged to ensure that software and hardware advances can be simultaneously achieved.

Advances in Characterization
The materials investigation activities will require novel in-situ material characterization equipment and methods with very high temporal and spatial resolutions to reveal the microscopic picture of physical dynamics.

D. Quantum Technology Hubs Desired End-State

The desired end-state is a commercial foundry-like access with fast turn-around times. Access to these fabrication facilities, which are amenable to developing process design kits (PDKs) for a variety of leading qubit types and support technologies, should be provided to DoD supported university/academic based collaborators as well as support the U.S. commercial quantum technology industry needs. Subsequently, fast tape-out schedules for academics and industry will both enhance the feedback time for established researchers and open the possibility for new groups or companies to better explore the landscape of qubit chip designs which may be viable for transitions to large scale implementations. The goal is to assist in the development of quantum processor quality and capability as well as quantum sensor and quantum network support. To achieve this end-state, multiple needs must be addressed.

Integration
Quantum technology requires specialized Systems on Chip (SoCs) that are capable of preparing, manipulating, and measuring quantum information as well as operating classical control algorithms to utilize that quantum information, all at the required fidelity and speed for technological advantage. Hubs will need to facilitate the advancement of multiple emerging microchip platforms, integration of those platforms, and novel test and measurement capability.

There are several quantum chip (QC) technologies being developed in the U.S. private sector that promise to scale to advantageous computational size including, but not limited to, superconducting quantum bits (qubits), semiconductor spins, ions, neutral atoms, solid state color centers and photons, each of which have several variations. These diverse technologies may have varying needs so it is not necessarily expected that one solution will be able support all possible quantum technologies; however, it is expected that solutions support the multiple needs of the QC technologies proposed.

Quantum Technology hubs are not meant to support the direct "scaling up" of quantum computing technologies to compute size of economic advantage. This is a matter for quantum computing companies to address using advancements made within the MEC Quantum Computing hubs. The hubs are meant to advance the capabilities of the micro fabricated quantum chips and SoCs that this emerging sector need to advance more quickly. Therefore, at this time, Government funding from this call will not be applied to quantum computing chips projects with more than 200 physical qubits. This constraint may change in the future as quantum computing power increases. Innovative solutions are requested to achieve the following advances:

Advances in Emerging Platforms and Materials
Quantum technology and especially quantum computing technology is built on a collection of emerging micro fabricated platforms including superconducting platforms, high band-gap photonics, non-linear optical materials, and other specialized materials. The acceleration of research in some of the leading qubit types is still hampered by lack of reliable access to these high-quality materials. Examples include clean superconducting materials with high surface quality, isotopically purified silicon-28, and materials like diamond or SiC that can host defect color centers. Some qubits also required engineered hybrid superconducting/semiconducting materials. Establishing formal channels and/or processes for acquiring these materials will speed up research progress.

These platforms can have fabrication and packaging requirements that differ from other microelectronics. For example, large temperature cycling between fabrication, often at high temperature to improve surface roughness, and operation, often at cryogenic temperatures, present a significant challenge. The emerging quantum ecosystem requires advances in these emerging platforms to realize the potential of quantum technology.

Advances in Quantum Support Chips and Integration
These specialized QCs are not thought to operate alone, but will need support from "classical" microchips that are themselves specialized. QCs, depending somewhat on the type of qubits onboard, need integrated transistor logic, monolithic microwave integrated circuits (MMIC), and photonic integrated circuits (PIC) operating at shorter wavelengths. These Quantum Systems of Chip (Q-SoCs) will require advances in these support chips as well as three-dimensional integration and packaging techniques. This integration will be all the more difficult because the qubits on QCs are typically fragile and susceptible to stray electromagnetic fields. Specific examples include developing multilayer, microwave-integrated, three-dimensional microwave heterostructures for superconducting qubits, integration of cryogenic CMOS with qubits, and integration of PICs with with high bandwidth and high extinction to address atomic systems or color centers. Quantum sensors, of many types also need access to integrated photonics components and, separately, superconductor material that may be distinct from qubits for computing.

Advances in Test and Measurement Capability
QCs are difficult to characterize because they must be operated in a regime where quantum effects become apparent (for example in vacuum or at low temperature) and those quantum effects may present unique observation challenges.

Other Desired Outcomes
It is desired that the hubs will have access to non-quantum based electronics experts outside of quantum physics. Additional desired outcomes of Quantum Technology hubs include, but are not limited to, the following demonstrations: 1) cryogenic quantum systems with classical electronics; 2) photonic integrated circuits with gain, low loss, and non-linear device sections on one platform; 3) integrated single photon detectors and high-flux, high-fidelity entangled photon sources; and 4) on-chip quantum information transduction between different qubit types (e.g., superconductors and optical photons).

While applicable to all hubs, it is re-highlighted here that some of these capabilities may be immature and may not be immediately available so it is expected that any hub have the ability to be upgradable with novel materials and fabrication techniques as material and technology capabilities improve over time.

E. Electromagnetic Warfare Hubs Desired End-State

The future of Electromagnetic Warfare (EW) reflects a paradigm shift from the traditional approach of deploying disparate systems to perform singular functions within a rigid spectrum allocation. Modern EW (Radar, Electronic Support Measurers, Electronic Attack, and Electronic Protection) requires rapid deployment of capabilities to outpace the threat using force-level, multi-function systems with ability to sense presence of targets and threats using all of the Electromagnetic Spectrum (EMS).

The desired end-state is lab-to-fab maturation of prototypes to support EW, as well as other EMS activities, existing primarily in the application space consuming digitized data from multi-platform sensors and transmitting via programmable multi-function apertures. Hubs will facilitate lab-to-fab maturation of critical microelectronic technologies and applications for transmit, receive, digitization, transport, and processing of received EMS signals for EW missions.

Those EM and EMS activities described above are enabled by Domain-Specific Systems-on-Chip (DSSoCs) and discrete chips providing electronic survivability, electronic attack, and electronic support at

a wider range of operating frequencies, instantaneous bandwidths, and resolution/bit-depth. All of this must be accomplished with improved form factor and thermal efficiency for DoD to gain technological advantage.

There are several EW relevant chip ideas being developed in the commercial sector including, but not limited to, high frequency RF digital to analog converters (DACs/ADCs), RF systems on chip (RFSoCs), digital readout integrated circuits (DROICs), AI-accelerating hardware, high-speed networking, ultra-wide bandgap semiconductors for both RF and power, and simultaneous transmit and receive (STAR) that can bring EW system-level performance down to package scale.

While the commercial sector technologies show relevance, additional lab-to-fab maturation efforts of ME and support electronics are required to ensure that technology satisfies stringent military requirements. In addition, military devices often operate at higher power and higher temperatures as compared to those used in the commercial sector. Improvements are required for domestic foundries to support existing high temperature materials and increase the transistor per chip area capability. Lab-to-fab prototype demonstrations to achieve the following advances are needed:

Advances in Emerging Platforms
EW technology and especially EW edge (edge defined as literally at an edge of a sensor system, or the most forward platform in combat operations) computing technology is currently built predominantly on commercially available field programmable gate arrays (FPGAs), precluding a fundamental technology advantage for the U.S. In addition, these components and sub-systems can have tight form factor requirements that differ from other microelectronics such as conformality, higher temperature, shock, and vibration.

Platform signal and data processing must rapidly and efficiently combine all sources of information into a coherent and manageable interface for both weapon systems and human operators. The ability to rapidly apply Artificial Intelligence/Machine Learning (AI/ML) algorithms across the broad expanses of the Electromagnetic (EM) environment will be essential for removing the ambiguities of the complexity expected in future environments. AI/ML chips will be needed to assist weapon systems and human operators manage the volume of information being received. An automated means to make sense of data streams and to remove clearly redundant information will be required.

Directed Energy (DE) Electronics
The DoD requires advanced microelectronics for non-kinetic directed energy weapons. Lab-to-fab solutions such as those producing state-of-the-art electrical performances in high-voltage fast-opening switches, beam control, microwave and mmW RF microelectronics, pulsed power of electromagnetic energy, and others for DE applications are critical to defend U.S. interests.

Advances in Support Electronics
Application specific EW chips do not operate independently from support electronics such as filters, power, control, status, and calibration/timing devices, which in their own right are specialized and serve as primary contributors to EMS sensor SWaP. Onboard logic, RF, and power electronics will vary at both the chip and package level as a function of architecture and platform constraints. Systems-in-Package (EW-SiPs) will require lab-to-fab maturation of these support electronics.

Examples of support electronics and their impact on performance include 1) compact tunable high performance filters to enable high performance across the EMS, 2) innovations in DC-to-DC converters enable increased power densities with improvements to efficiencies, and 3) built-in measurement, built-in test, and calibration electronics enabling confidence in system mission readiness and optimized performance.

Heterogeneous Integration

The emerging domestic EW-specific electronics ecosystem requires advances in packaging design tools and approaches in order to fully realize leading edge device technologies while maintaining separation from commercially competitive application spaces. However, 2.5D/3D heterogeneous integration efforts are being supported through other DoD and USG investments. Therefore, at this time, 2.5D/3D heterogeneous integration should not be a focus of the Electronic Warfare hubs.

F. Commercial Leap Ahead Technologies Hubs Desired End State

Commercial leap ahead technologies are innovative technologies in which the commercial industry has little to no *current* business interests that warrant their investment. These leap ahead technologies fall under one of two categories: 1) technologies that provide revolutionary capabilities, and 2) designs of systems that allow us to insert new technologies that will yield dramatically new capabilities.[1]

The desired end state is the lab-to-fab maturation of materials, devices, architectures, and processes to provide and/or enable revolutionary capabilities. Desired end-states may include but are not limited to:

Integration of Technologies with CMOS
In what has recently been termed CMOS+X, X represents a broad array of technologies; both the Quantum Technology and AI Hardware Sections include descriptions of needed CMOS+X advancements. The "X" includes but is not limited to spintronics, memristors, ferroelectrics, and for example, topological materials. Submissions are requested that advance the integration of emerging materials with existing industry standard microchip platforms. As an expanded example, submissions are requested which advance progress towards topologically enabled systems on chips (SoCs) that are capable of acquiring, processing and storing the large data sets required, e.g., for battlespace sensing/surveillance and the internet of the battlefield, which achieve significant power reduction and increased speed over conventional systems at the required fidelity for technological advantage. Solutions should also advance the integration of emerging topological devices and materials with existing industry standard microchip platforms.

Advances in the High-Power Wide Bandgap Devices Ecosystem
Wide bandgap and ultra-wide bandgap technologies offer significant SWaP and efficiency payoff for converters and RF systems. Consideration will be given for lab-to-fab demonstration of devices and processes for wide bandgap gallium nitride, SiC, gallium oxide, and diamond. Advances in these emerging technologies will realize the potential of wide bandgap and ultra-wide bandgap power devices.

Advances in SOI Wafer Manufacturing and Wafer Bonding
Develop on-shore state-of-the-art SOI wafer manufacturing in a trusted environment. Develop a trusted manufacturing flow for production-level manufacture and processing of radiation-hardened ultra-thin body and box (UTBB) SOI wafers. Develop trusted flow for handling radiation-hardened wafers from manufacture to final device fabrication at a domestic facility.

Research Fabrication Hub for Leap Ahead Technologies
The desired end state is a capability to fabricate on-demand nanometer, heterogeneous, complex structures using dielectric, metal, semiconductor and/or other emerging materials. The objective is to fabricate, characterize and test structures, devices and circuits with new electronic, electro-optic (for

[1] "Leap Ahead Technologies and Transformation Initiatives within the Defense Science and Technology Program", Hearing before the Subcommittee on Emerging Threats and Capabilities of the Committee on Armed Services, United States Senate, June 05, 2001.

example, optics integrated as components for compute and communication applications) or quantum functionality that can be rapidly transitioned to commercial foundries.

Optoelectronics Leap Ahead
The desired end-state(s) are prototypes that lead to the adoption and integration of revolutionary, capability-enabling (i) material platforms and their manufacturing, (ii) methods for power delivery and dissipation, and (iii) operational modalities that leap ahead of existing commercial optoelectronic products towards new concepts of operation (CONOPS) at higher performance and/or efficiency. Hubs will facilitate developments into micro-electronic and micro-optoelectronic devices comprised of revolutionary materials and advanced power management solutions that go beyond established solutions available in the commercial sector in one or more performance metrics.

Advances in Emergent Material Platforms
Expanding the fundamental capabilities of sensors, computing architectures, and memory storage at reduced SWaP requires manufacturing improvements for high-yield, low-defect processing of new material systems in place of traditional semiconductor platforms. Poor quality wafer scale growth at manufacturing volume of candidate optoelectronic material alternatives, such as two-dimensional materials (e.g., molybdenum disulfide), semiconductor alloys (e.g., silicon germanium tin), and/or low dimensional crystals (e.g., quantum dots) have largely precluded realization of commercial devices that leverage their full technological potential. Other emergent material systems with potential for domestic sourcing in raw elemental, molecular, or mineral form and high-purity refinement techniques are of interest to strengthen supply chain availability for microelectronics. Domestic sourcing and synthesis of high quality, new material platforms is a fundamental precursor to innovative device designs with new degrees of freedom.

Advances in Standardization of Hybrid Optical-Electrical Signal Processing Architectures
Signal processing and computing devices built upon electronic integrated circuitry, and, more recently, PIC, are built upon standardized, analogous components (e.g., resistors vs. waveguides) that allow a common toolset for designing new products. Hybrid devices built upon open systems architecture concepts with data-fused electronic and photonic constituents can strategically leverage the strengths of each to execute signal processing tasks on-chip, including artificial intelligence and neural networks, towards actionable data to circumvent user judgement/interpretation. However, further innovations are required to standardize the design toolset of hybrid circuitry devices to balance speed, SWaP, and data fidelity. Other approaches to embedded, intelligent processing beyond the traditional serialized detector-processor-algorithm approach could provide competitive opportunities.

Advances in Power Management
Fielding of distributed, fused sensor networks in the Internet of Battlefield Things (IoBT) with practical SWaP requires innovations in power delivery concepts and embedded thermal management schemes. Prototyping opportunities exist for integrating solid-state energy harvesting concepts for sustained operations. Existing thermal management approaches to electrical processing devices, especially in nanometer-scale node technologies, govern their performance (e.g., clock speed) and SWaP. New materials, devices, and architectures can be demonstrated via packaging schemes that incorporate innovative heat rejection and dissipation concepts to circumvent traditional SWaP penalties of adding conductive thermal mass and/or convective heat exchangers.